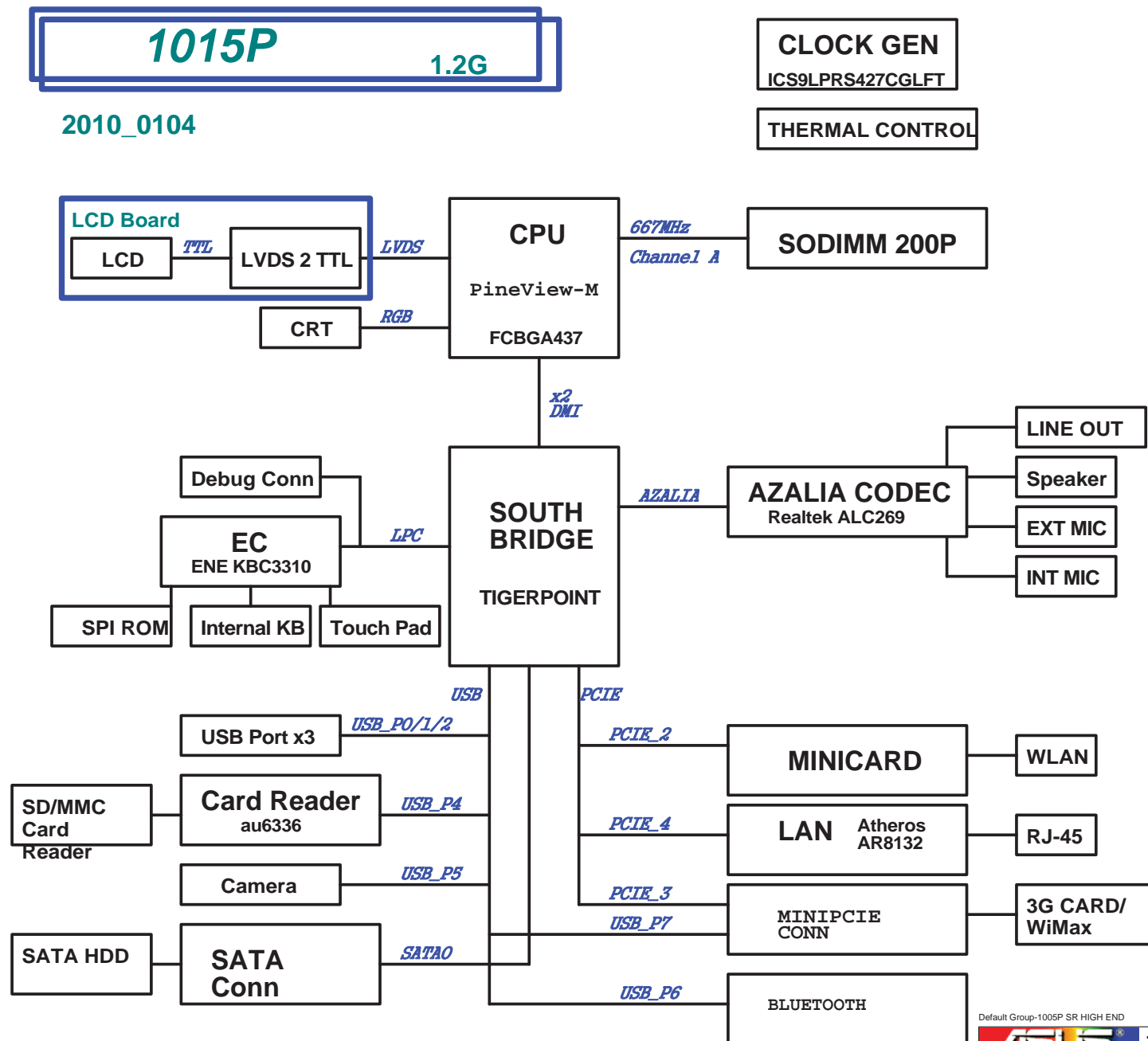


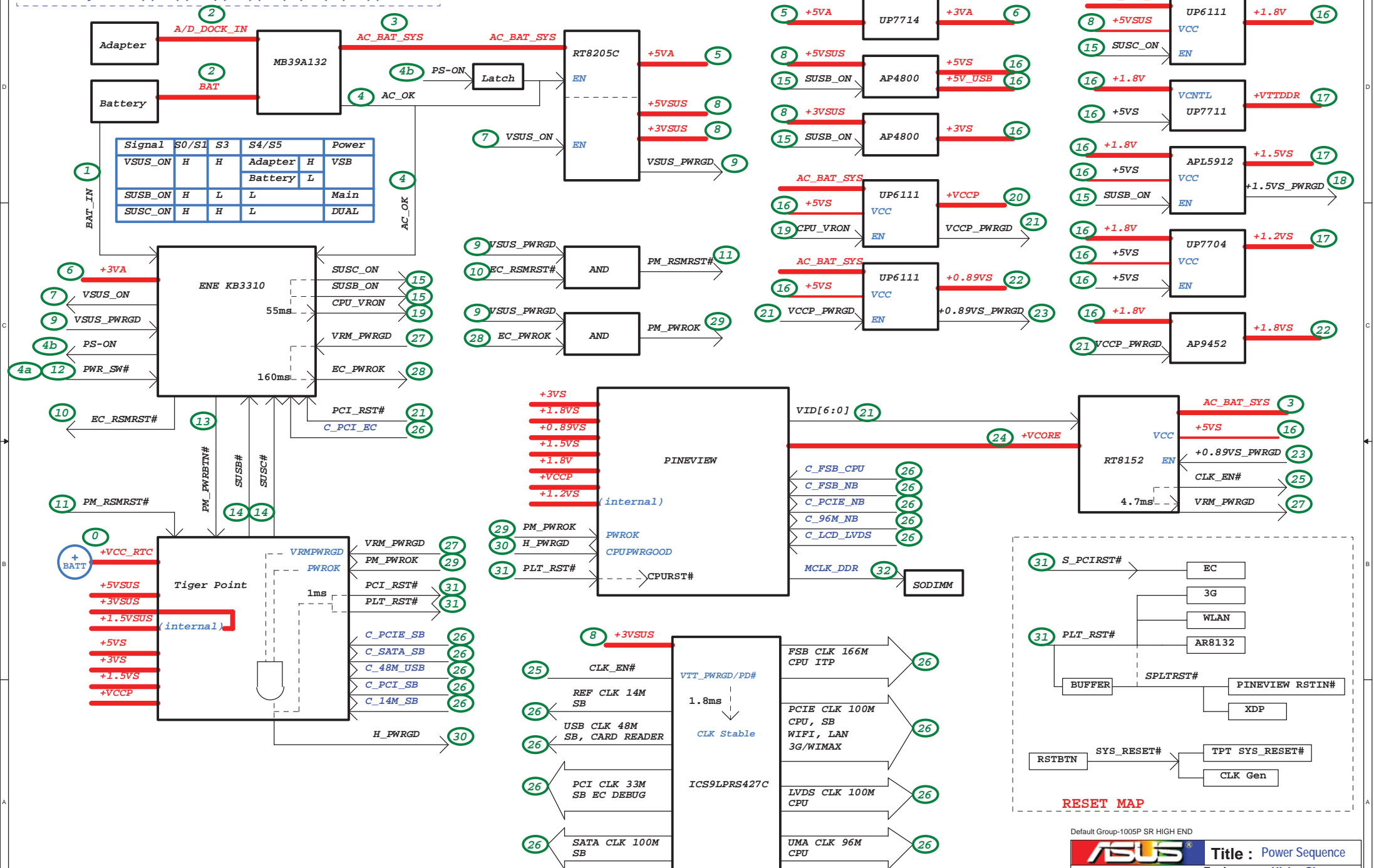
01.Block Diagram
02.Power Sequence
03.Clock Gen_ICS9LPRS427C
04.PineView-M_1 (LVDS_DMI_CPU)
05.PineView-M_2 (DDR2_XDP_CRT)
06.PineView-M_3 (PWR&GND)
07.XDP
08.Tigerpoint_DMI_USB
09.Tigerpoint_SYS
10.Tigerpoint_PWR
11.DDR2 SODIMM
12.DDR2-Termination
13.Onboard VGA
14.LCD Conn_LID
15.WIFI&SMART33SW
16.LAN_AR8132
17.WLAN
18.USIN&3G_CON
19.Bluetooth
20.HDD_CON
21.
22.
23.USB Port1
24.EC_ENE KB3310
25.KB_TP
26.Fan_debug
27.SPI_ROM
28.DUA_CON
29.PWR Jack
30_Discharge
31.
32.Srew Hole&EMI
33.Power Flow
34.Power_Charger
35.Vcore
36.Power_+1.8V&VTDDR&+1.8VS
37.Power_VCCP
38.Power_+0.89VS
39.Power_+1.5VS
40.Power Latch
41.Power System
42.power switch



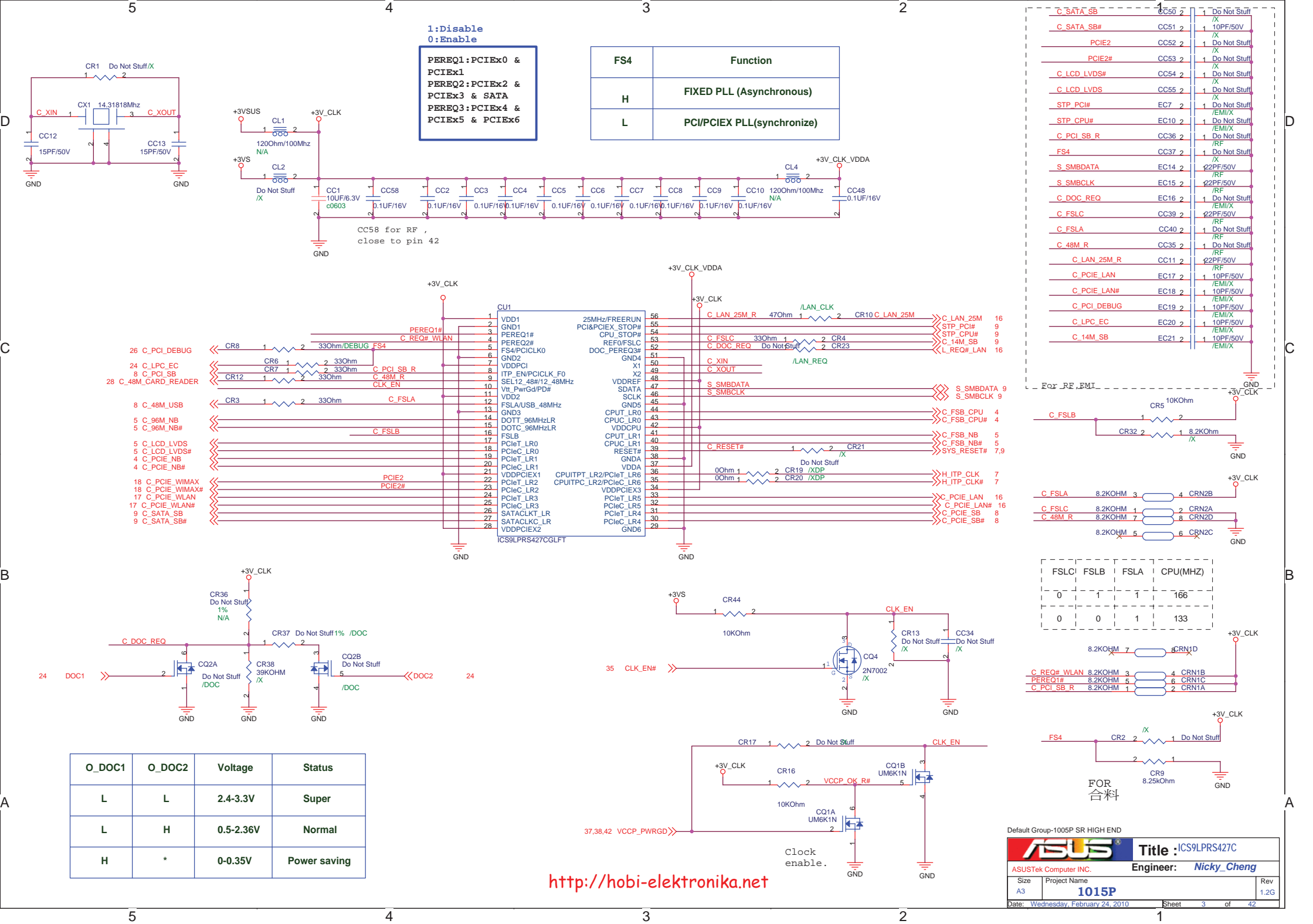
Default Group-1005P SR HIGH END

ASUS		Title : Block Diagram	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size Custom	Project Name 1015P	Rev 1.2G	
Date: Wednesday, February 24, 2010		Sheet 1 of 42	

For Adapter Mode: (1) -> (2) -> (3) -> (4) -> (5) -> ...
For Battery Mode: (1) -> (2) -> (3) -> (4) -> (4a) -> (4b) -> (5) -> ...



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11 D2_MAA[14:0]

D2_MAA0 AH19
D2_MAA1 AJ18
D2_MAA2 AK18
D2_MAA3 AK16
D2_MAA4 AJ14
D2_MAA5 AH14
D2_MAA6 AK14
D2_MAA7 AJ12
D2_MAA8 AH13
D2_MAA9 AK12
D2_MAA10 AK20
D2_MAA11 AH12
D2_MAA12 AJ11
D2_MAA13 AJ24
D2_MAA14 AJ24

NU1C

DDR_A_MA_0
DDR_A_MA_1
DDR_A_MA_2
DDR_A_MA_3
DDR_A_MA_4
DDR_A_MA_5
DDR_A_MA_6
DDR_A_MA_7
DDR_A_MA_8
DDR_A_MA_9
DDR_A_MA_10
DDR_A_MA_11
DDR_A_MA_12
DDR_A_MA_13
DDR_A_MA_14

DDR_A_DQS_0
DDR_A_DQS_1
DDR_A_DQS_2
DDR_A_DQS_3
DDR_A_DQS_4
DDR_A_DQS_5
DDR_A_DQS_6
DDR_A_DQS_7

DDR_A_DQ_0
DDR_A_DQ_1
DDR_A_DQ_2
DDR_A_DQ_3
DDR_A_DQ_4
DDR_A_DQ_5
DDR_A_DQ_6
DDR_A_DQ_7

DDR_A_DQ_8
DDR_A_DQ_9
DDR_A_DQ_10
DDR_A_DQ_11
DDR_A_DQ_12
DDR_A_DQ_13
DDR_A_DQ_14
DDR_A_DQ_15

DDR_A_CS_0
DDR_A_CS_1
DDR_A_CS_2
DDR_A_CS_3

DDR_A_CKE_0
DDR_A_CKE_1
DDR_A_CKE_2
DDR_A_CKE_3

DDR_A_ODT_0
DDR_A_ODT_1
DDR_A_ODT_2
DDR_A_ODT_3

DDR_A_DQS_3
DDR_A_DQS_4
DDR_A_DQS_5
DDR_A_DQS_6

DDR_A_DQ_3
DDR_A_DQ_4
DDR_A_DQ_5
DDR_A_DQ_6

DDR_A_DQ_7
DDR_A_DQ_8
DDR_A_DQ_9
DDR_A_DQ_10

DDR_A_DQ_11
DDR_A_DQ_12
DDR_A_DQ_13
DDR_A_DQ_14

DDR_A_DQ_15
DDR_A_DQ_16
DDR_A_DQ_17
DDR_A_DQ_18

DDR_A_DQ_19
DDR_A_DQ_20
DDR_A_DQ_21
DDR_A_DQ_22

DDR_A_DQ_23
DDR_A_DQ_24
DDR_A_DQ_25
DDR_A_DQ_26

DDR_A_DQ_27
DDR_A_DQ_28
DDR_A_DQ_29
DDR_A_DQ_30

DDR_A_DQ_31
DDR_A_DQ_32
DDR_A_DQ_33
DDR_A_DQ_34

DDR_A_DQ_35
DDR_A_DQ_36
DDR_A_DQ_37
DDR_A_DQ_38

DDR_A_DQ_39
DDR_A_DQ_40
DDR_A_DQ_41
DDR_A_DQ_42

DDR_A_DQ_43
DDR_A_DQ_44
DDR_A_DQ_45
DDR_A_DQ_46

DDR_A_DQ_47
DDR_A_DQ_48
DDR_A_DQ_49
DDR_A_DQ_50

DDR_A_DQ_51
DDR_A_DQ_52
DDR_A_DQ_53
DDR_A_DQ_54

DDR_A_DQ_55
DDR_A_DQ_56
DDR_A_DQ_57
DDR_A_DQ_58

DDR_A_DQ_59
DDR_A_DQ_60
DDR_A_DQ_61
DDR_A_DQ_62

DDR_A_DQ_63
DDR_A_DQ_64
DDR_A_DQ_65
DDR_A_DQ_66

MICRO-FCBGA8-559
N/A

AD3 D2_DQS_A0
AD2 D2_DQS_A#0
AD4 D2_DM_A0
AC4 D2_DQ_A0
AC1 D2_DQ_A1
AF4 D2_DQ_A2
AG2 D2_DQ_A3
AB2 D2_DQ_A4
AB3 D2_DQ_A5
AE2 D2_DQ_A6
AE3 D2_DQ_A7

AB8 D2_DQS_A1
AD7 D2_DQS_A#1
AA9 D2_DM_A1
AB6 D2_DQ_A8
AB7 D2_DQ_A9
AE5 D2_DQ_A10
AG5 D2_DQ_A11
AA5 D2_DQ_A12
AB5 D2_DQ_A13
AB8 D2_DQ_A14
AD6 D2_DQ_A15

AD8 D2_DQS_A2
AD10 D2_DQS_A#2
AE8 D2_DM_A2
AG8 D2_DQ_A16
AG7 D2_DQ_A17
AE10 D2_DQ_A18
AG11 D2_DQ_A19
AE7 D2_DQ_A20
AE8 D2_DQ_A21

AD11 D2_DQ_A22
AE10 D2_DQ_A23
AK5 D2_DQS_A3
AK3 D2_DQS_A#3
AJ3 D2_DM_A3
AH1 D2_DQ_A24
AJ2 D2_DQ_A25

AK6 D2_DQ_A26
AJ7 D2_DQ_A27
AF3 D2_DQ_A28
AH2 D2_DQ_A29
AL5 D2_DQ_A30
AJ6 D2_DQ_A31
AG22 D2_DQS_A4
AG21 D2_DQS_A#4

AD19 D2_DM_A4
AE19 D2_DQ_A32
AG19 D2_DQ_A33
AF22 D2_DQ_A34
AD22 D2_DQ_A35
AG17 D2_DQ_A36
AF19 D2_DQ_A37
AE21 D2_DQ_A38
AD21 D2_DQ_A39

AE26 D2_DQS_A5
AG27 D2_DQS_A#5
AJ27 D2_DM_A5
AE24 D2_DQ_A40
AG25 D2_DQ_A41
AD25 D2_DQ_A42
AD24 D2_DQ_A43
AG22 D2_DQ_A44

AG24 D2_DQ_A45
AD27 D2_DQ_A46
AE27 D2_DQ_A47
AE30 D2_DQS_A6
AF29 D2_DQS_A#6
AF30 D2_DM_A6

AG31 D2_DQ_A48
AG30 D2_DQ_A49
AD30 D2_DQ_A50
AD29 D2_DQ_A51
AJ30 D2_DQ_A52
AJ29 D2_DQ_A53
AE29 D2_DQ_A54
AD28 D2_DQ_A55

AB27 D2_DQS_A7
AA27 D2_DQS_A#7
AB26 D2_DM_A7
AA24 D2_DQ_A56
AB25 D2_DQ_A57
W22 D2_DQ_A58
W24 D2_DQ_A59
AB24 D2_DQ_A60

AB23 D2_DQ_A61
AA23 D2_DQ_A62
W27 D2_DQ_A63
AB27 D2_DQS_A7
AA27 D2_DQS_A#7
AB26 D2_DM_A7
AA24 D2_DQ_A56

AB25 D2_DQ_A57
W22 D2_DQ_A58
W24 D2_DQ_A59
AB24 D2_DQ_A60
AB23 D2_DQ_A61
AA23 D2_DQ_A62
W27 D2_DQ_A63

AB27 D2_DQS_A7
AA27 D2_DQS_A#7
AB26 D2_DM_A7
AA24 D2_DQ_A56
AB25 D2_DQ_A57
W22 D2_DQ_A58
W24 D2_DQ_A59

AB24 D2_DQ_A60
AB23 D2_DQ_A61
AA23 D2_DQ_A62
W27 D2_DQ_A63
AB27 D2_DQS_A7
AA27 D2_DQS_A#7
AB26 D2_DM_A7

AA24 D2_DQ_A56
AB25 D2_DQ_A57
W22 D2_DQ_A58
W24 D2_DQ_A59
AB24 D2_DQ_A60
AB23 D2_DQ_A61
AA23 D2_DQ_A62

W27 D2_DQ_A63
AB27 D2_DQS_A7
AA27 D2_DQS_A#7
AB26 D2_DM_A7
AA24 D2_DQ_A56
AB25 D2_DQ_A57
W22 D2_DQ_A58

W24 D2_DQ_A59
AB24 D2_DQ_A60
AB23 D2_DQ_A61
AA23 D2_DQ_A62
W27 D2_DQ_A63
AB27 D2_DQS_A7
AA27 D2_DQS_A#7

AB26 D2_DM_A7
AA24 D2_DQ_A56
AB25 D2_DQ_A57
W22 D2_DQ_A58
W24 D2_DQ_A59
AB24 D2_DQ_A60
AB23 D2_DQ_A61

AA23 D2_DQ_A62
W27 D2_DQ_A63
AB27 D2_DQS_A7
AA27 D2_DQS_A#7
AB26 D2_DM_A7
AA24 D2_DQ_A56
AB25 D2_DQ_A57

W22 D2_DQ_A58
W24 D2_DQ_A59
AB24 D2_DQ_A60
AB23 D2_DQ_A61
AA23 D2_DQ_A62
W27 D2_DQ_A63
AB27 D2_DQS_A7

AA27 D2_DQS_A#7
AB26 D2_DM_A7
AA24 D2_DQ_A56
AB25 D2_DQ_A57
W22 D2_DQ_A58
W24 D2_DQ_A59
AB24 D2_DQ_A60

AB23 D2_DQ_A61
AA23 D2_DQ_A62
W27 D2_DQ_A63
AB27 D2_DQS_A7
AA27 D2_DQS_A#7
AB26 D2_DM_A7
AA24 D2_DQ_A56

AB25 D2_DQ_A57
W22 D2_DQ_A58
W24 D2_DQ_A59
AB24 D2_DQ_A60
AB23 D2_DQ_A61
AA23 D2_DQ_A62
W27 D2_DQ_A63

AB27 D2_DQS_A7
AA27 D2_DQS_A#7
AB26 D2_DM_A7
AA24 D2_DQ_A56
AB25 D2_DQ_A57
W22 D2_DQ_A58
W24 D2_DQ_A59

AB24 D2_DQ_A60
AB23 D2_DQ_A61
AA23 D2_DQ_A62
W27 D2_DQ_A63
AB27 D2_DQS_A7
AA27 D2_DQS_A#7
AB26 D2_DM_A7

11 D2_MAA[14:0]

D2_DQ_A[63:0] 11
D2_DQS_A[7:0] 11
D2_DQS_A#7[7:0] 11
D2_DM_A[7:0] 11

PVR22 1 2 1KOhm XDP_RSVD5
PVR19 1 2 1KOhm XDP_RSVD9
PV26 1 2 1KOhm XDP_RSVD17
PVR20 1 2 1KOhm XDP_RSVD17
GND

XDP_RSVD[0]
XDP_RSVD[1]
XDP_RSVD[2]
XDP_RSVD[3]
XDP_RSVD[4]
XDP_RSVD[5]
XDP_RSVD[6]
XDP_RSVD[7]
XDP_RSVD[8]
XDP_RSVD[9]
XDP_RSVD[10]
XDP_RSVD[11]
XDP_RSVD[12]
XDP_RSVD[13]
XDP_RSVD[14]
XDP_RSVD[15]
XDP_RSVD[16]
XDP_RSVD[17]

RSVD18
RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
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RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
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RSVD_TP10
RSVD_TP11
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RSVD_TP11
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RSVD_TP13

RSVD_TP3
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RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
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RSVD_TP13

RSVD_TP3
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RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
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RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
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RSVD_TP11
RSVD_TP1
RSVD_TP14
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RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

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DDC CLK&DATA need 2.2K Pull
up to +3VS(Or may we can use
4.7K);connector side has
pull-up resistor.

NU1D

XDP_RSVD[0]
XDP_RSVD[1]
XDP_RSVD[2]
XDP_RSVD[3]
XDP_RSVD[4]
XDP_RSVD[5]
XDP_RSVD[6]
XDP_RSVD[7]
XDP_RSVD[8]
XDP_RSVD[9]
XDP_RSVD[10]
XDP_RSVD[11]
XDP_RSVD[12]
XDP_RSVD[13]
XDP_RSVD[14]
XDP_RSVD[15]
XDP_RSVD[16]
XDP_RSVD[17]

RSVD18
RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13

CRT_HSYNC
CRT_VSYNC
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_IRTN
CRT_DDC_DATA
CRT_DDC_CLK
DAC_IREF
REFCLKINP
REFCLKINN
REFSSCLKINP
REFSSCLKINN
HPL_CLKINN
HPL_CLKINP

M30 V_HSYNC R PVR21 1 2 150hm
M29 V_VSYNC R PVR18 1 2 150hm
N31 V_RED 13
P30 V_GREEN 13
P29 V_BLUE 13
N30 GND
L31 GND
L30 GND
P28 DACREFSET PVR27 1 2 6650HM 1%

C.96M_NB# 3
C.96M_NB# 3
C.LCD_LVDS# 3
C.LCD_LVDS# 3

PM_DPRSPLVR 9,35
PM_EXTTS1 PVR29 1 2 10KOhm IX
PM_EXTTS0 PVR30 1 2 10KOhm IX
K29 J30
L5 AA3
W8 W9
C.FSB_NB# 3
C.FSB_NB# 3
PVC9 10PF/50V IX
PVC10 10PF/50V IX

PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

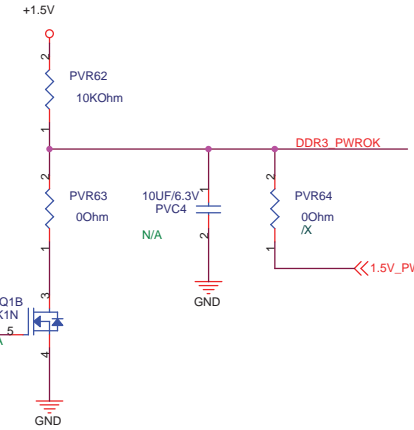
PM_EXTTS0
PM_EXTTS0 11

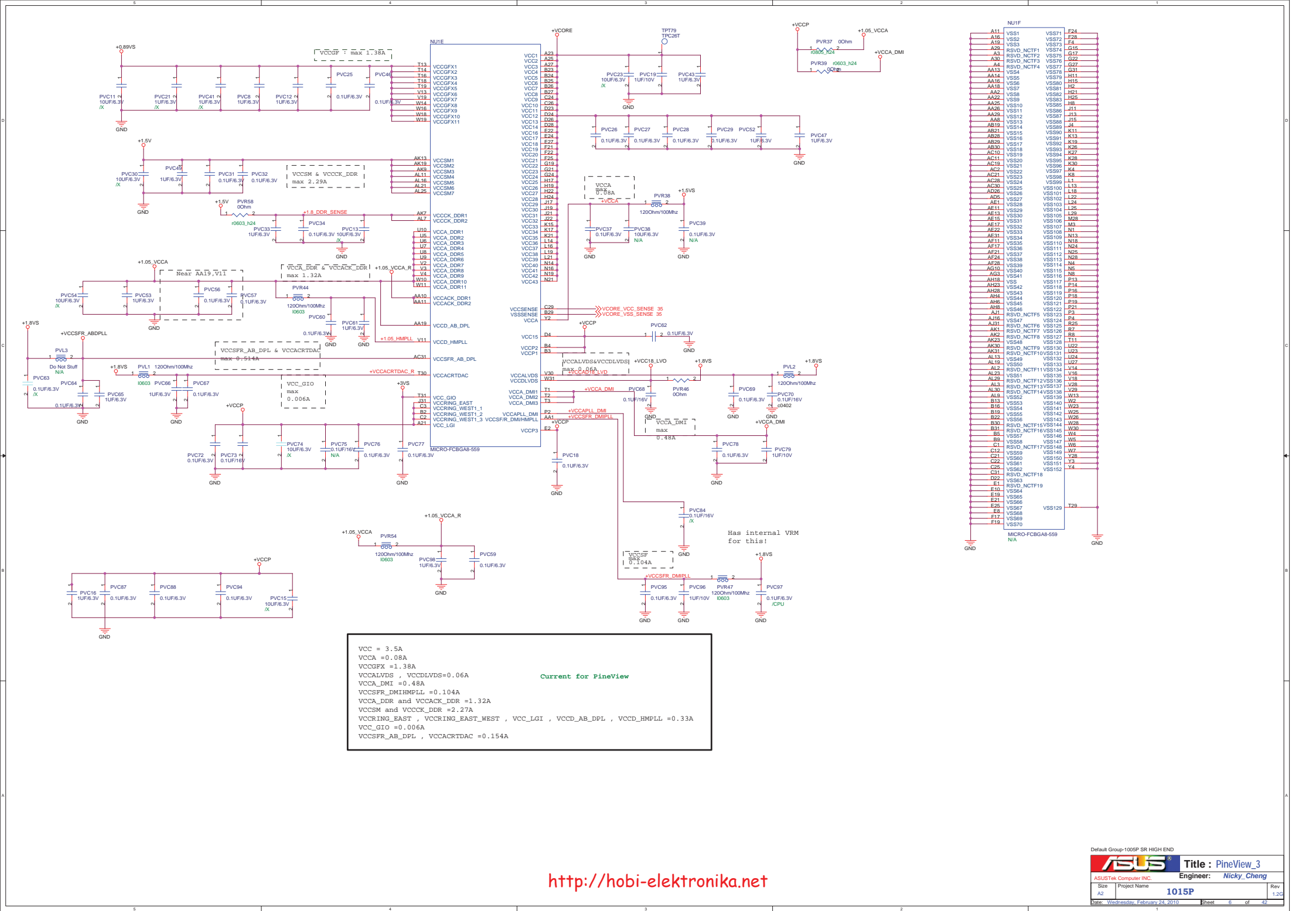
PM_EXTTS0
PM_EXTTS0 11

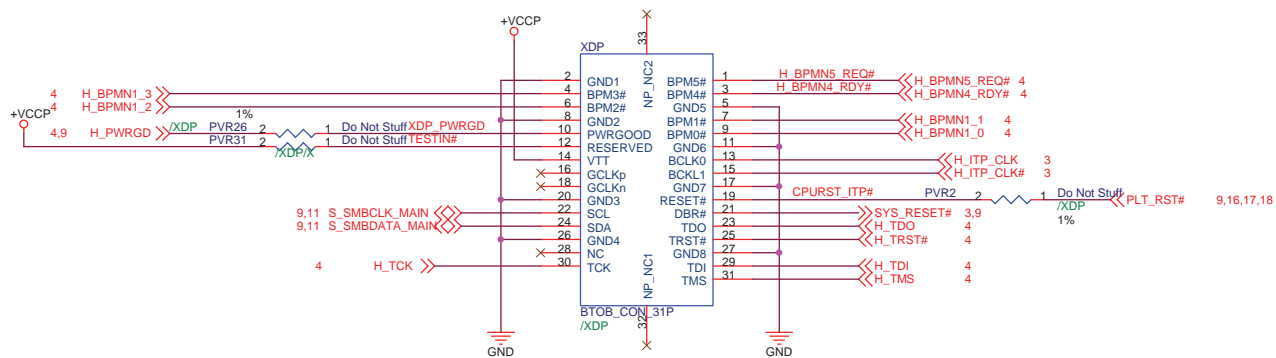
PM_EXTTS0
PM_EXTTS0 11

PM_EXTTS0
PM_EXTTS0 11

Intel confirm only RSVD9 need stuff 1K
resistor.







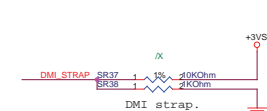
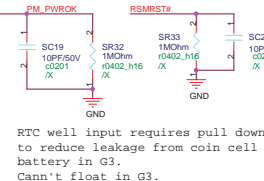
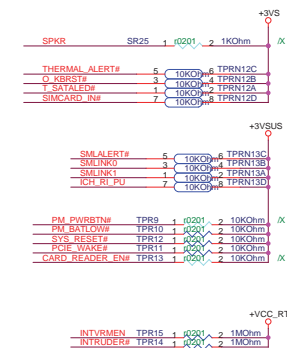
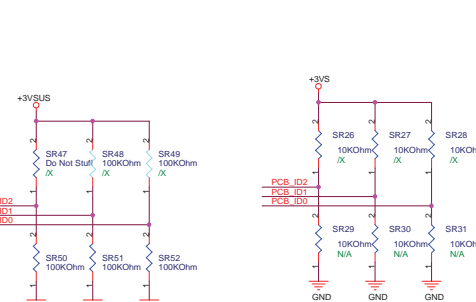
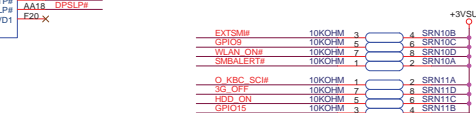
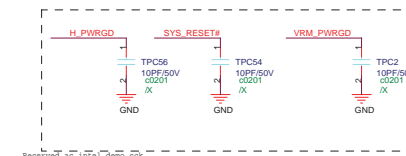
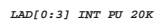
Change Device and PCB footprint of XDP1 to
nomask footprint - nomask solution

新 Layout 機種請 XDP Connector 請畫
12G161300311 (w/ 2 through holes)。



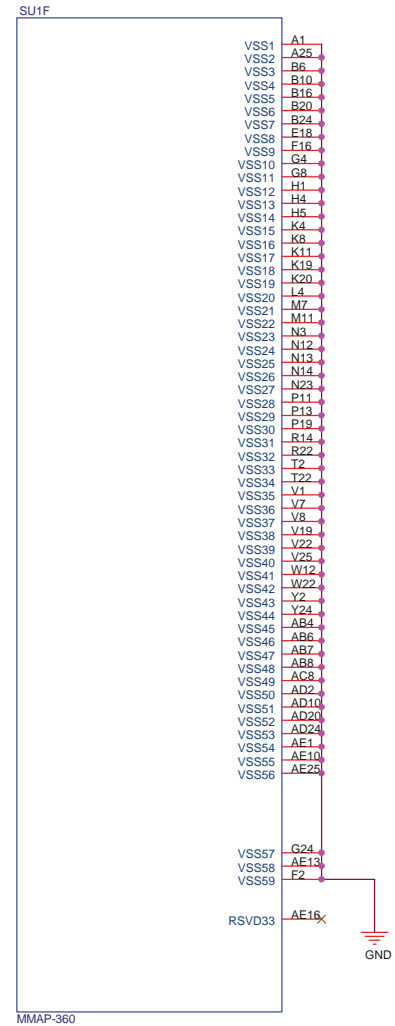
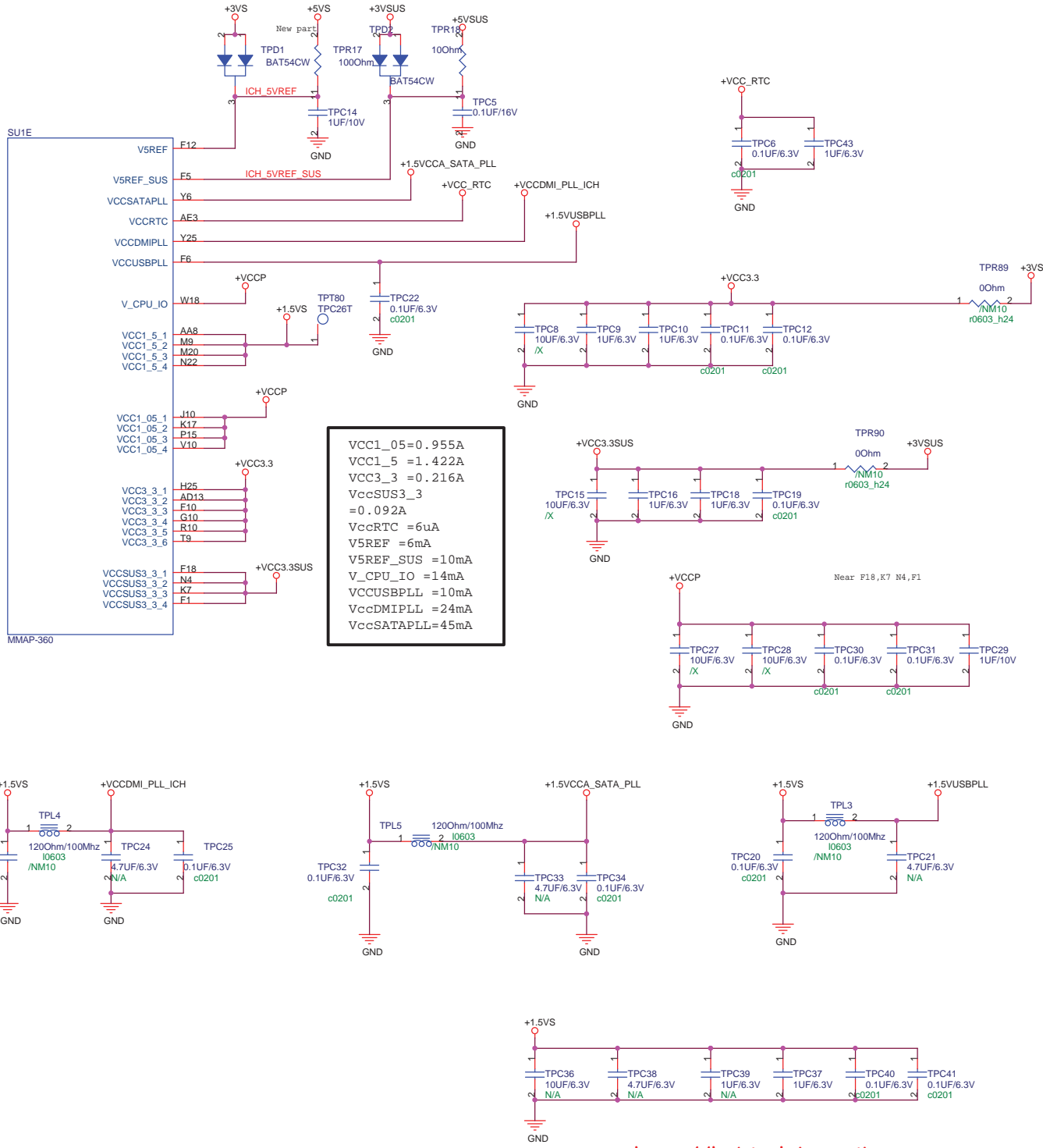


SATA RX,TX all need AC couple and place near Connector side for signal quality.And Traces to them should match length. ICH7M need pull down RX, if no use.



```
1=DMI interface is strapped to
operate in DC coupled mode.
0=DMI interface is strapped to
operate in AC coupled mode.
```


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<http://hobi-elektronika.net>

Default Group-1005P SR HIGH END

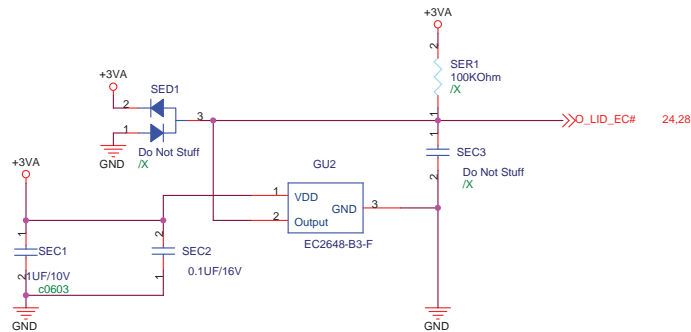
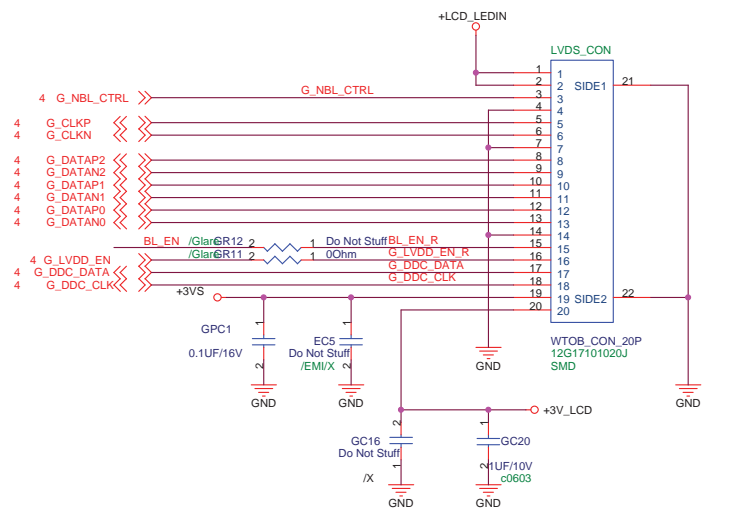


Title : **DDR3**

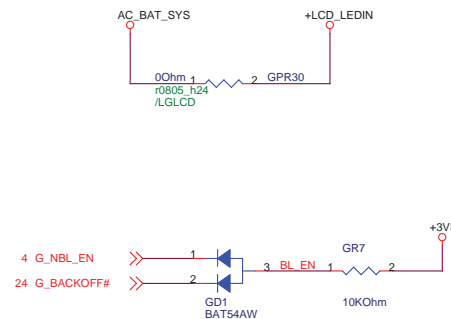
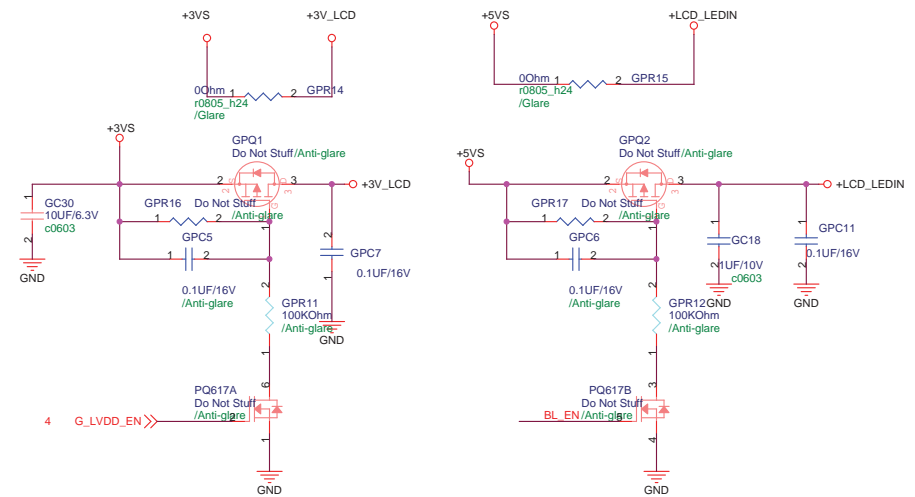
ASUSTek Computer INC. Engineer: **Nicky_Cheng**

Size	Project Name	Rev
A3	1015P	1.2G

Date: **Wednesday, February 24, 2010** Sheet **12** of **42**

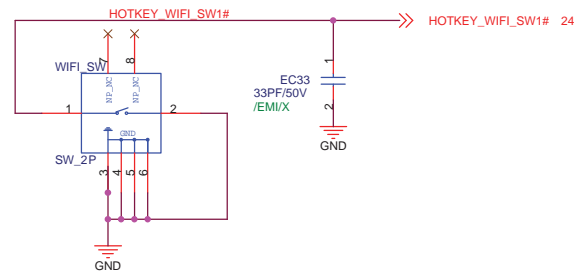
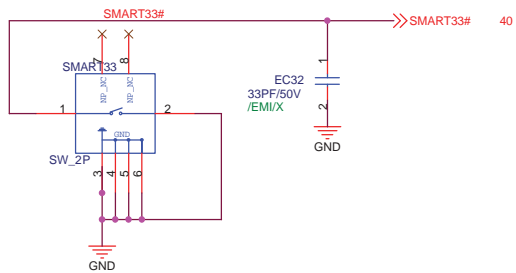


G_DDC_CLK	GC1	2	1	Do Not Stuff/X
G_DDC_DATA	GC2	2	1	Do Not Stuff/X
G_CLKP	GC3	2	1	10PF/50V EMI
G_CLKN	GC4	2	1	10PF/50V EMI
G_DATAP2	GC5	2	1	10PF/50V EMI
G_DATAN2	GC6	2	1	10PF/50V EMI
G_DATAP1	GC7	2	1	10PF/50V EMI
G_DATAN1	GC8	2	1	10PF/50V EMI
G_DATAP0	GC9	2	1	10PF/50V EMI
G_DATAN0	GC10	2	1	10PF/50V EMI
G_NBL_CTRL	GC12	2	1	Do Not Stuff/X
BL_EN	EC11	2	1	Do Not Stuff/EMI/X
G_LVDD_EN	EC12	2	1	Do Not Stuff/EMI/X



Default Group-1005P SR HIGH END

ASUS		Title : LVDS Conn_LID	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size Custom	Project Name 1015P	Rev 1.2G	
Date: Wednesday, February 24, 2010	Sheet	14	of 42



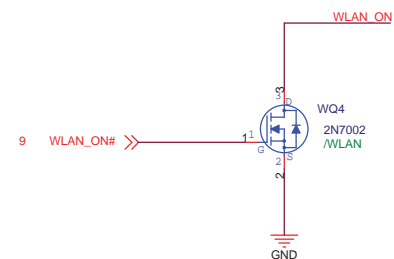
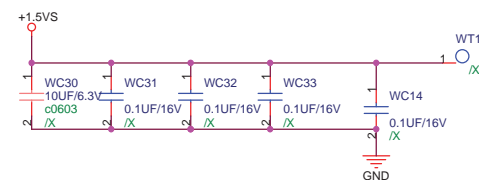
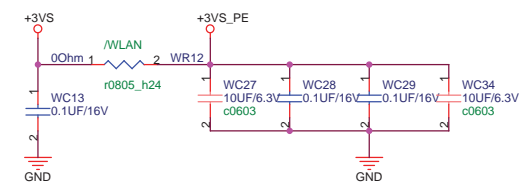
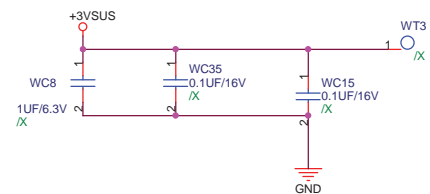
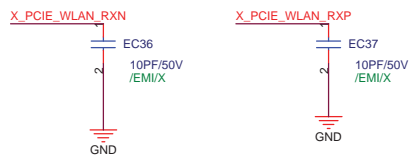
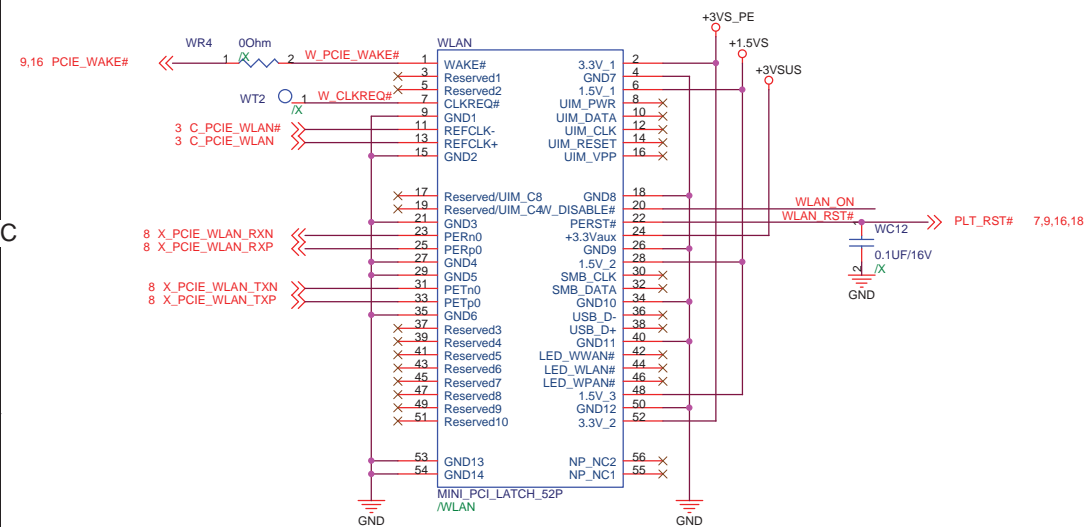
<http://hobi-elektronika.net>

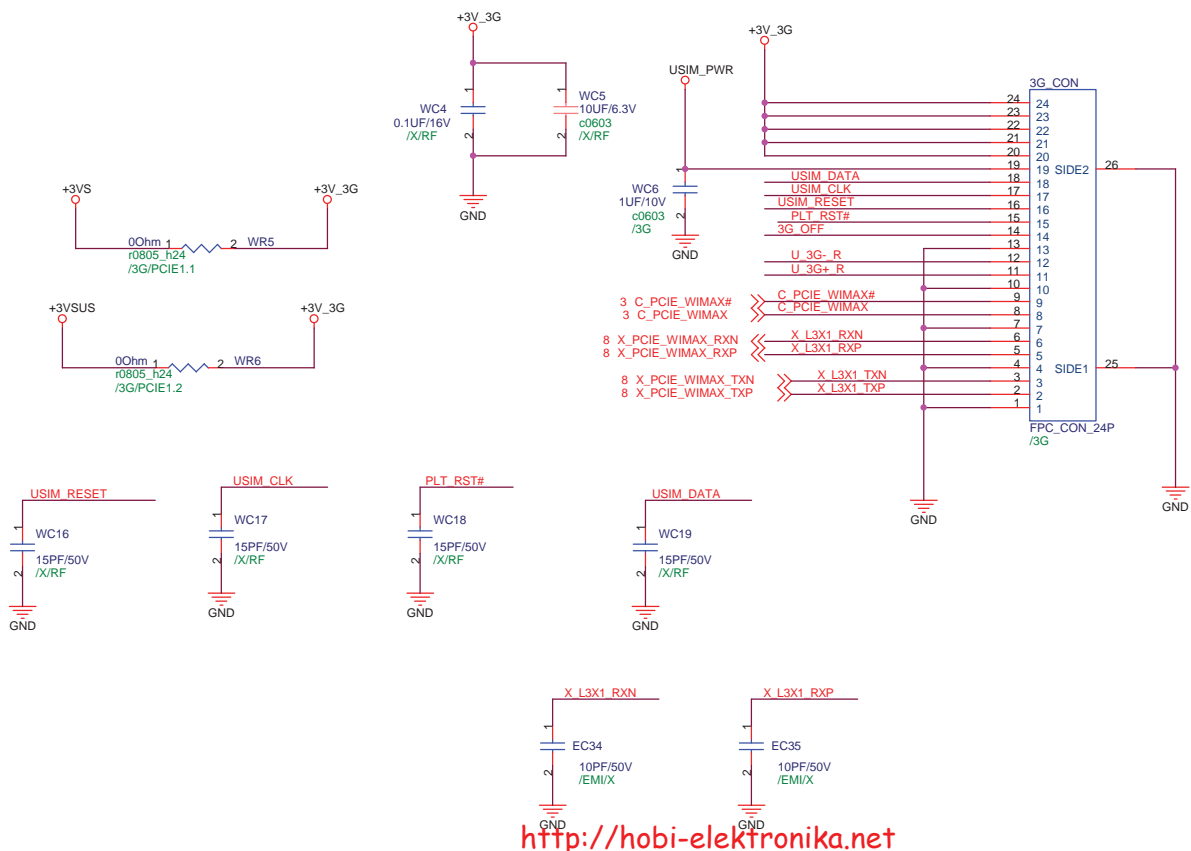
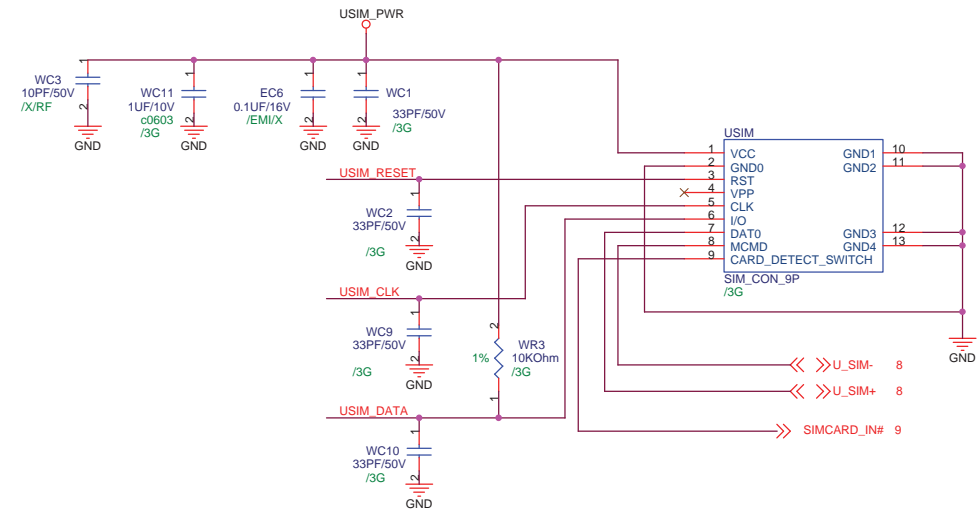
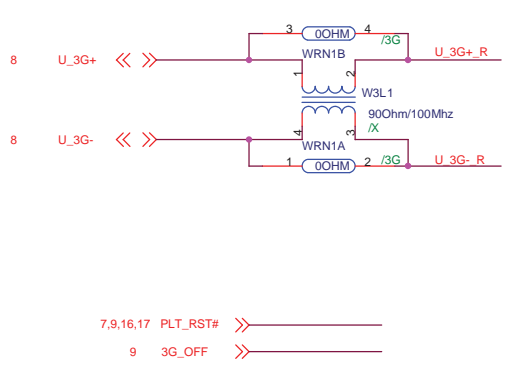
Default Group-1005P SR HIGH END

ASUS		Title : WIFI_SAMRT33	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size A3	Project Name 1015P	Rev 1.2G	
Date: Wednesday, February 24, 2010		Sheet 15 of 42	

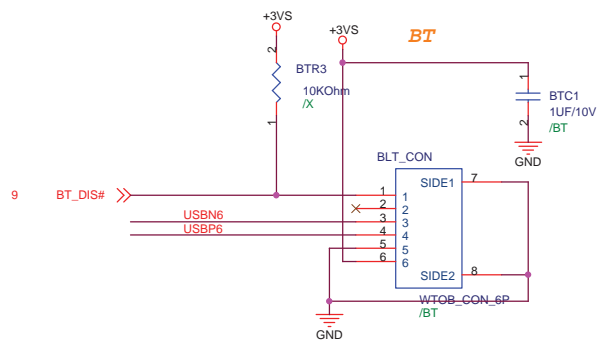
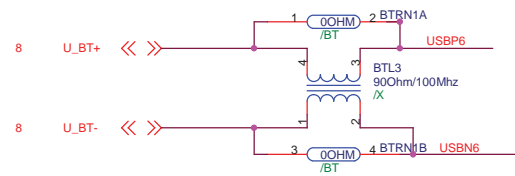


```
WIFI use PCIE 1.1 Spec
+3VS = 1.0A peak / 0.75A Normal
+1.5VS = 0.5A peak / 0.375A Normal
+3VSUS = 0.375A peak / 0.25A
Normal
```





<http://hobi-elektronika.net>

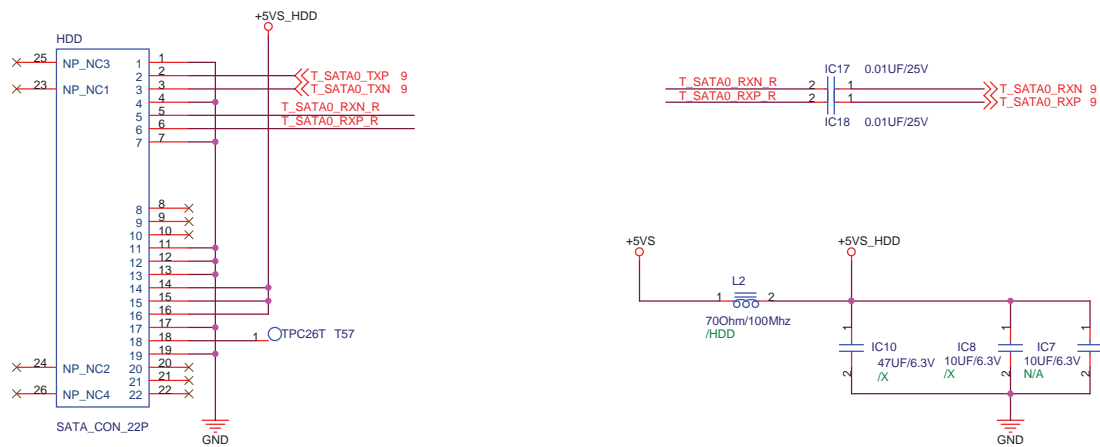


<http://hobi-elektronika.net>

Default Group-1005P SR HIGH END


ASUS		Title : Bluetooth	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size A3	Project Name 1015P	Rev 1.2G	
Date: Wednesday, February 24, 2010		Sheet 19	of 42

SATA HDD Connector

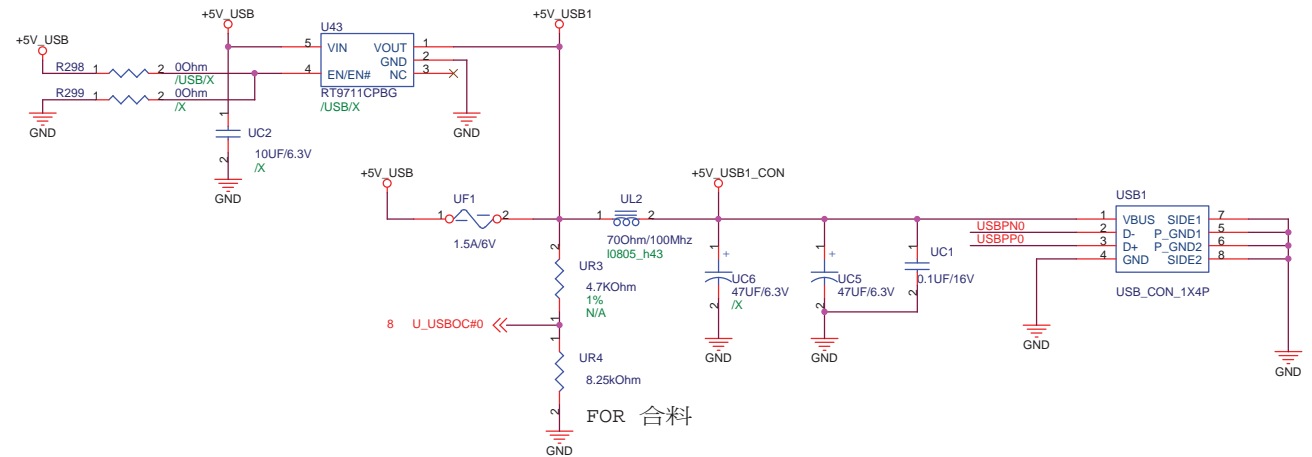
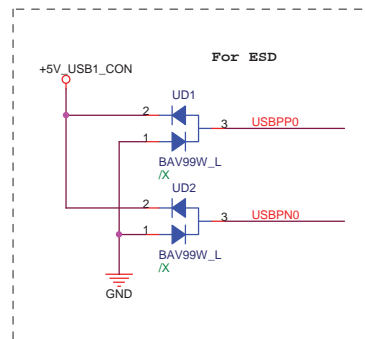
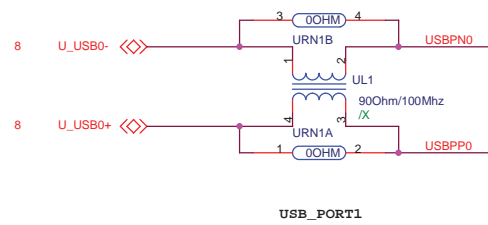


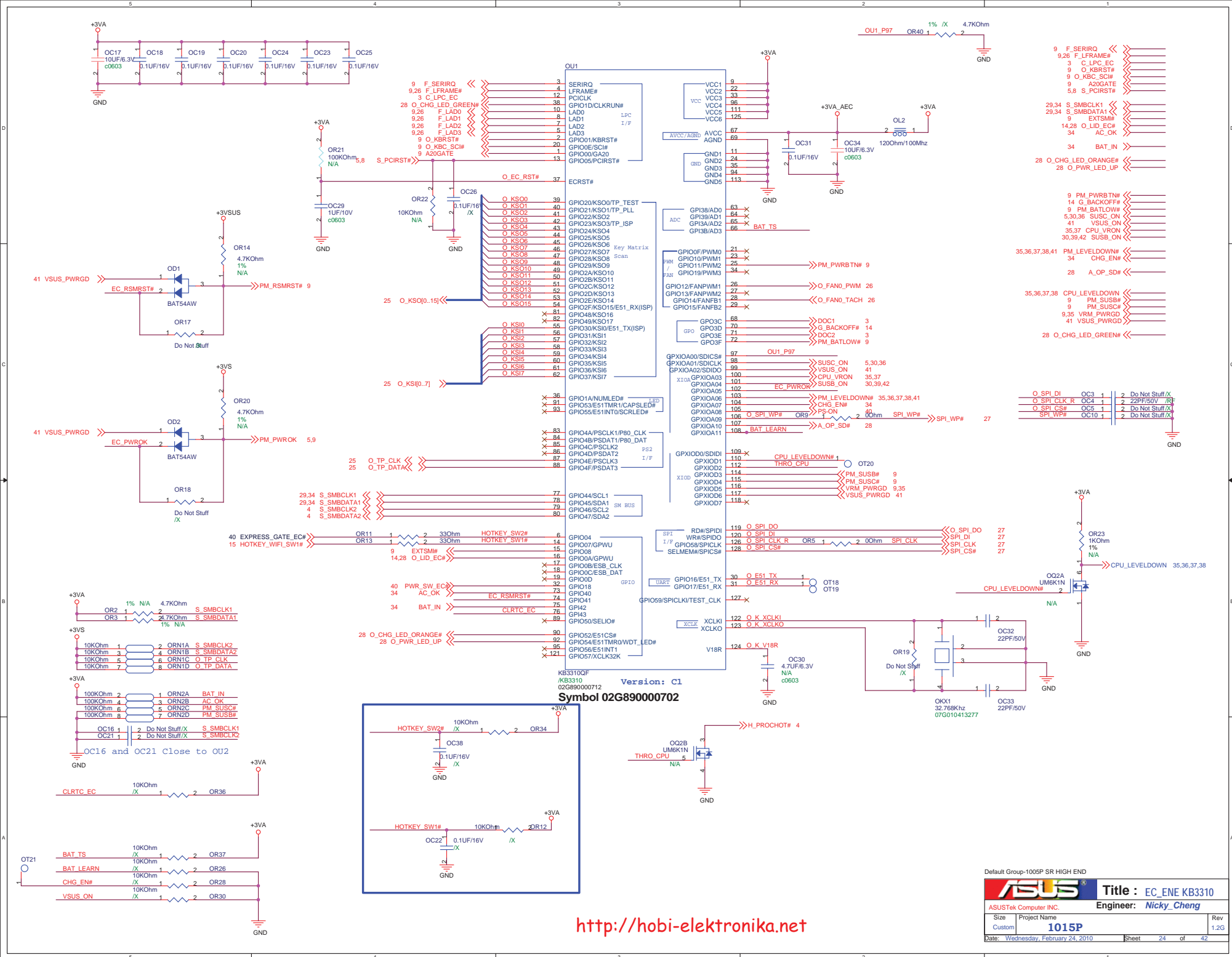


<http://hobi-elektronika.net>

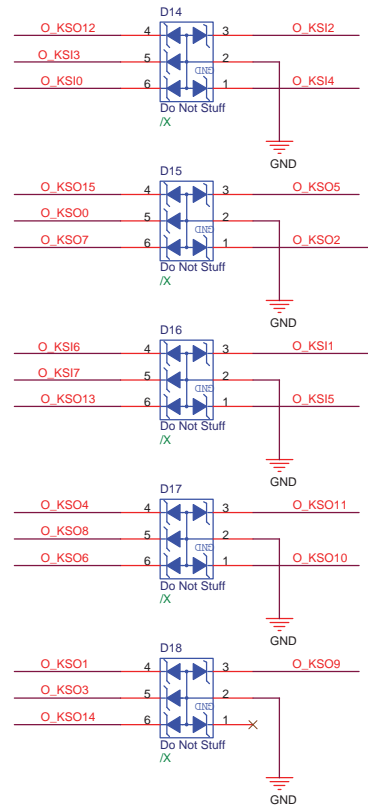
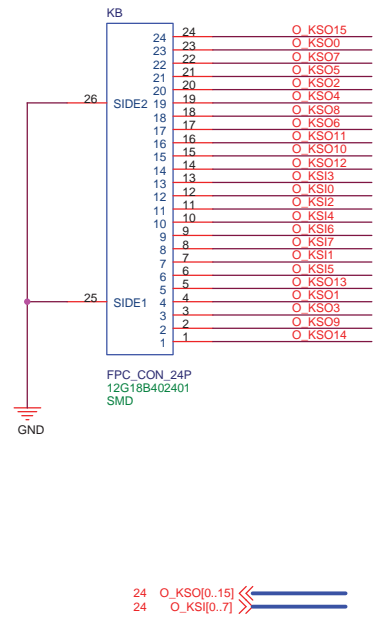
Default Group-1005P SR HIGH END		
		Title : USB3.0
ASUSTek Computer INC.		Engineer:
Size C	Project Name 1015P	Rev 1.2G
Date: Wednesday, February 24, 2010		Sheet 21 of 42



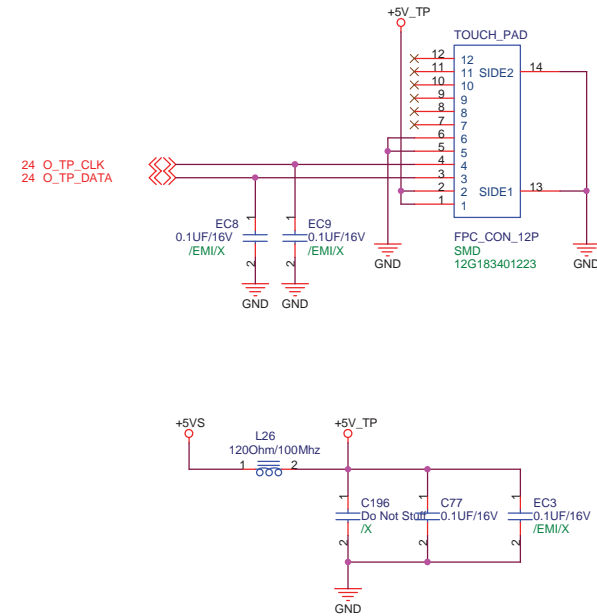


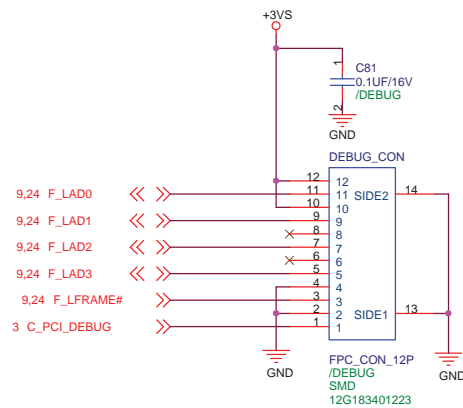
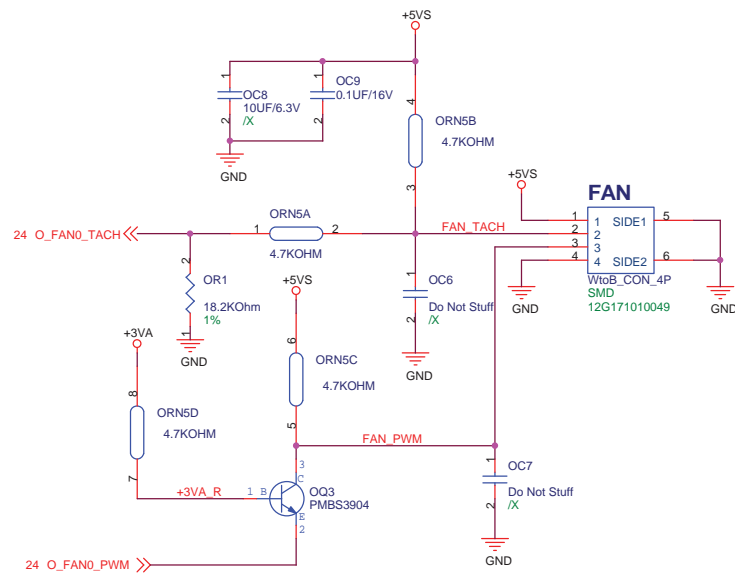


For Keyboard Connector

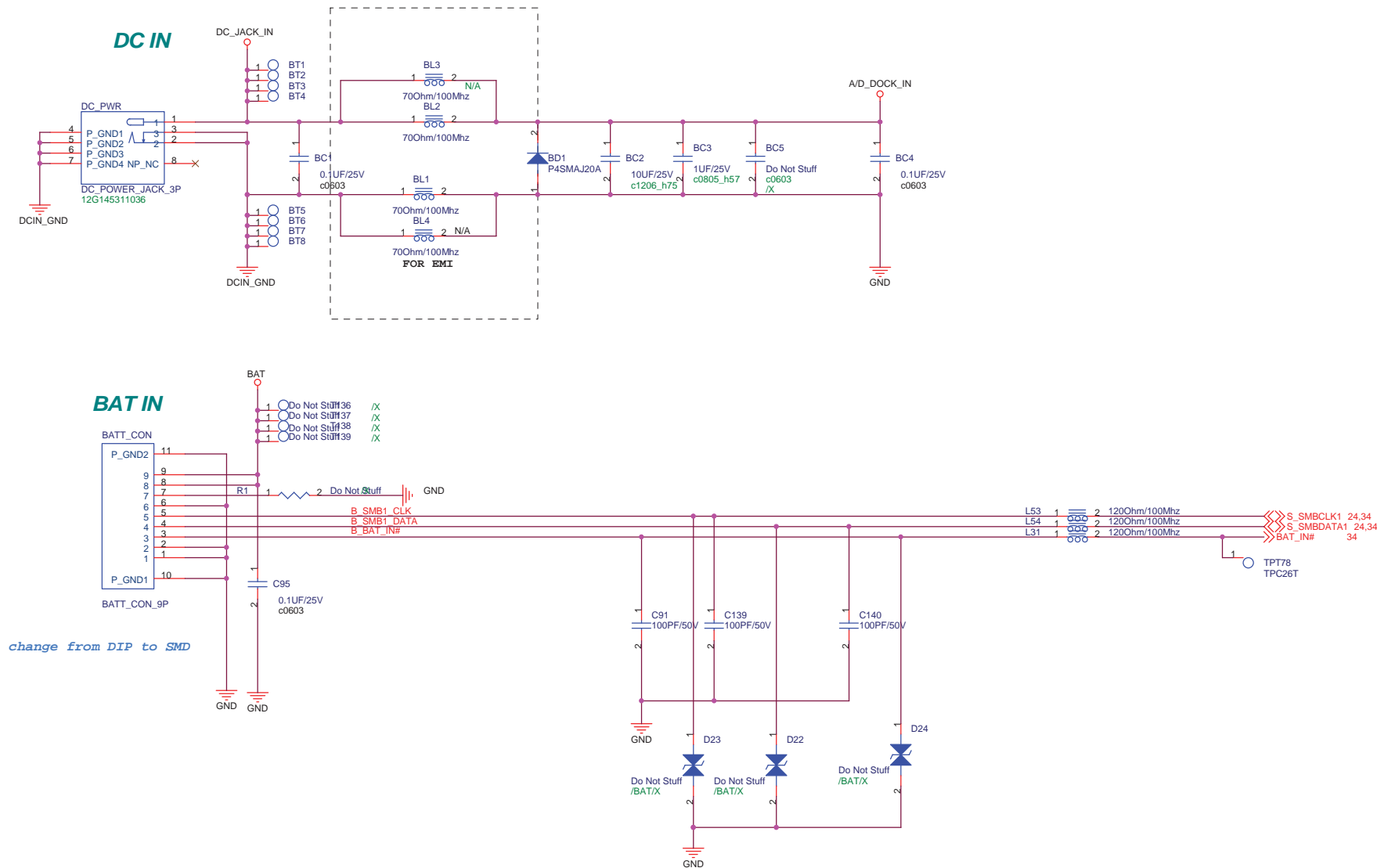


For Touch-Pad





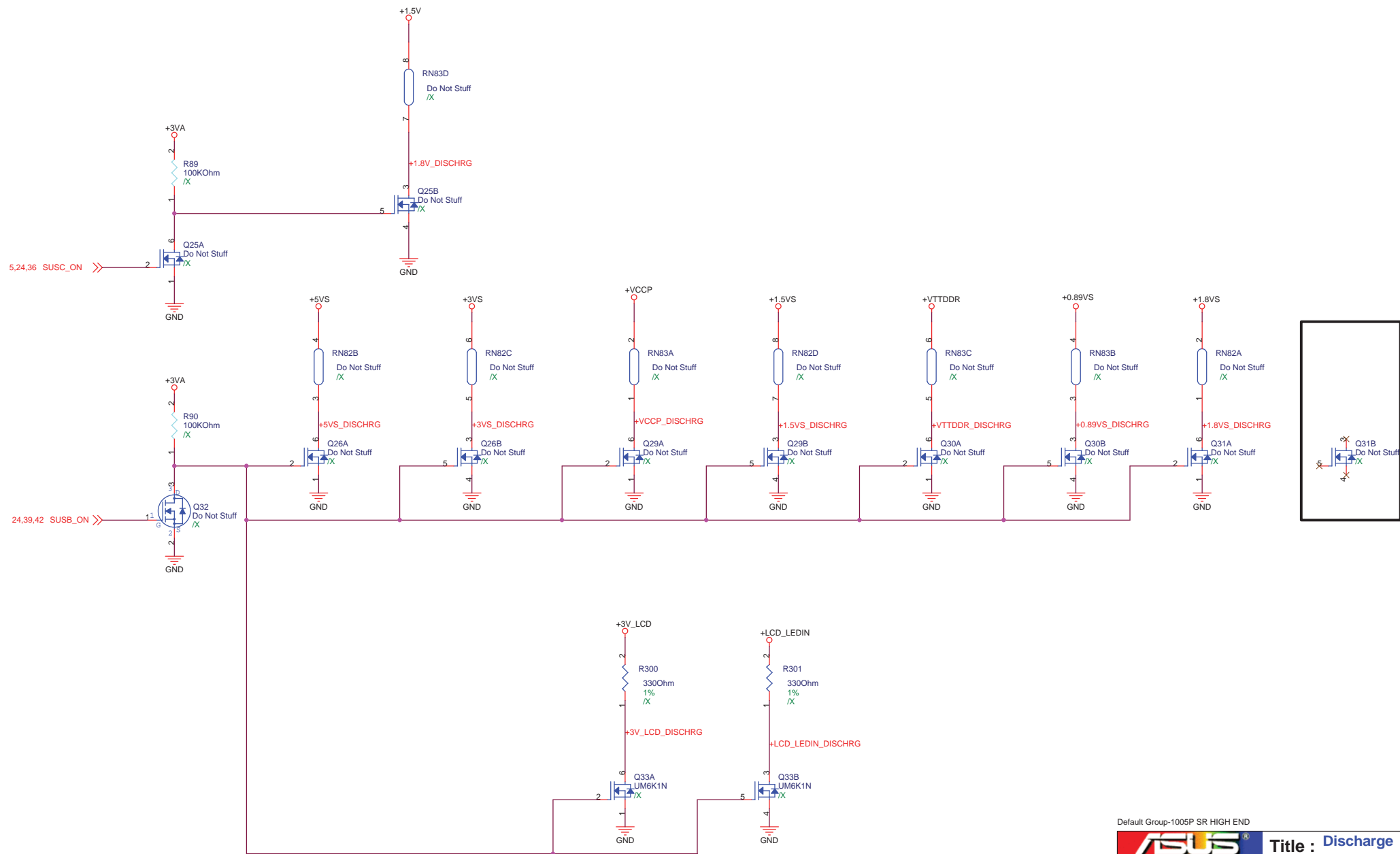
0.1B Beta



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Default Group-1005P SR HIGH END

ASUS		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size A3	Project Name 1015P	Rev 1.2G	
Date: Wednesday, February 24, 2010		Sheet 29 of 42	

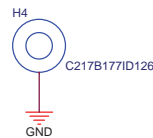
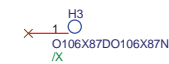
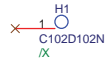
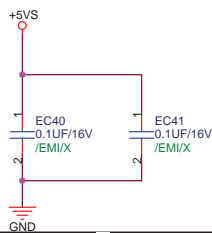
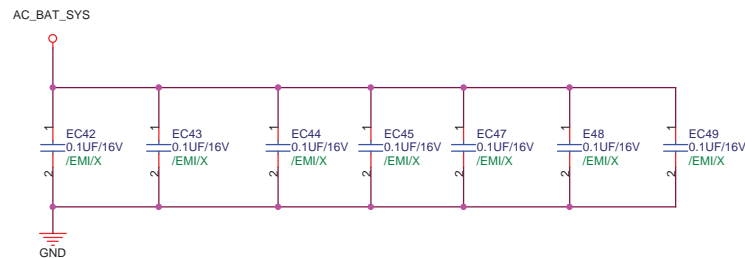
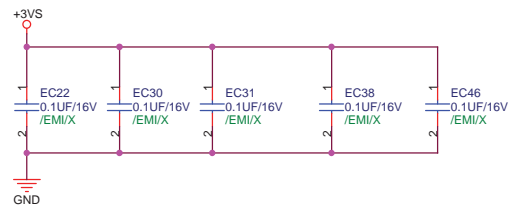
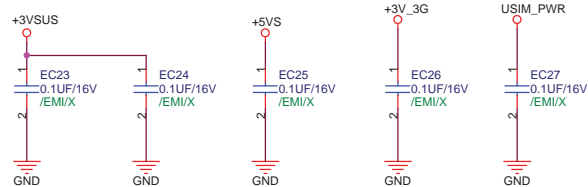
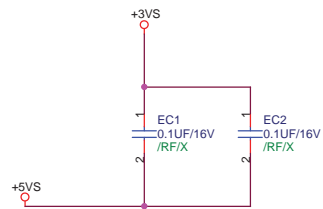


<http://hobi-elektronika.net>

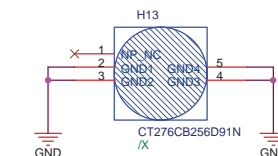
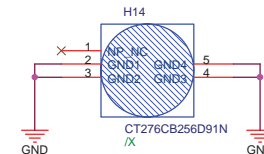
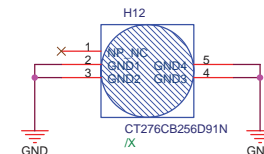
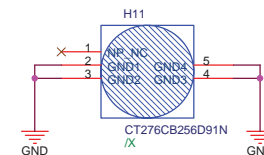
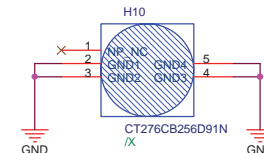
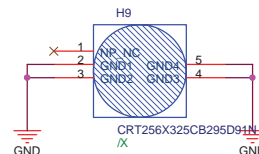
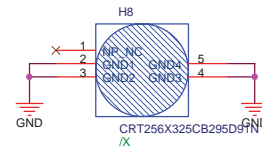
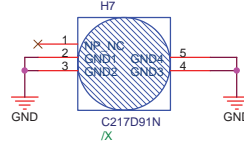
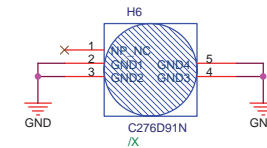
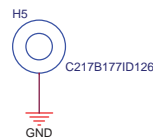
Default Group-1005P SR HIGH END

ASUS		Title : Discharge	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size A3	Project Name 1015P	Rev 1.2G	
Date: Wednesday, February 24, 2010	Sheet	30 of 42	

5	4	3	2	1
D				D
C				C
B				B
A				A



CPU Thermal HOLD



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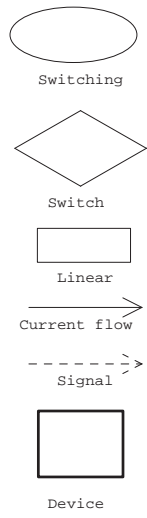
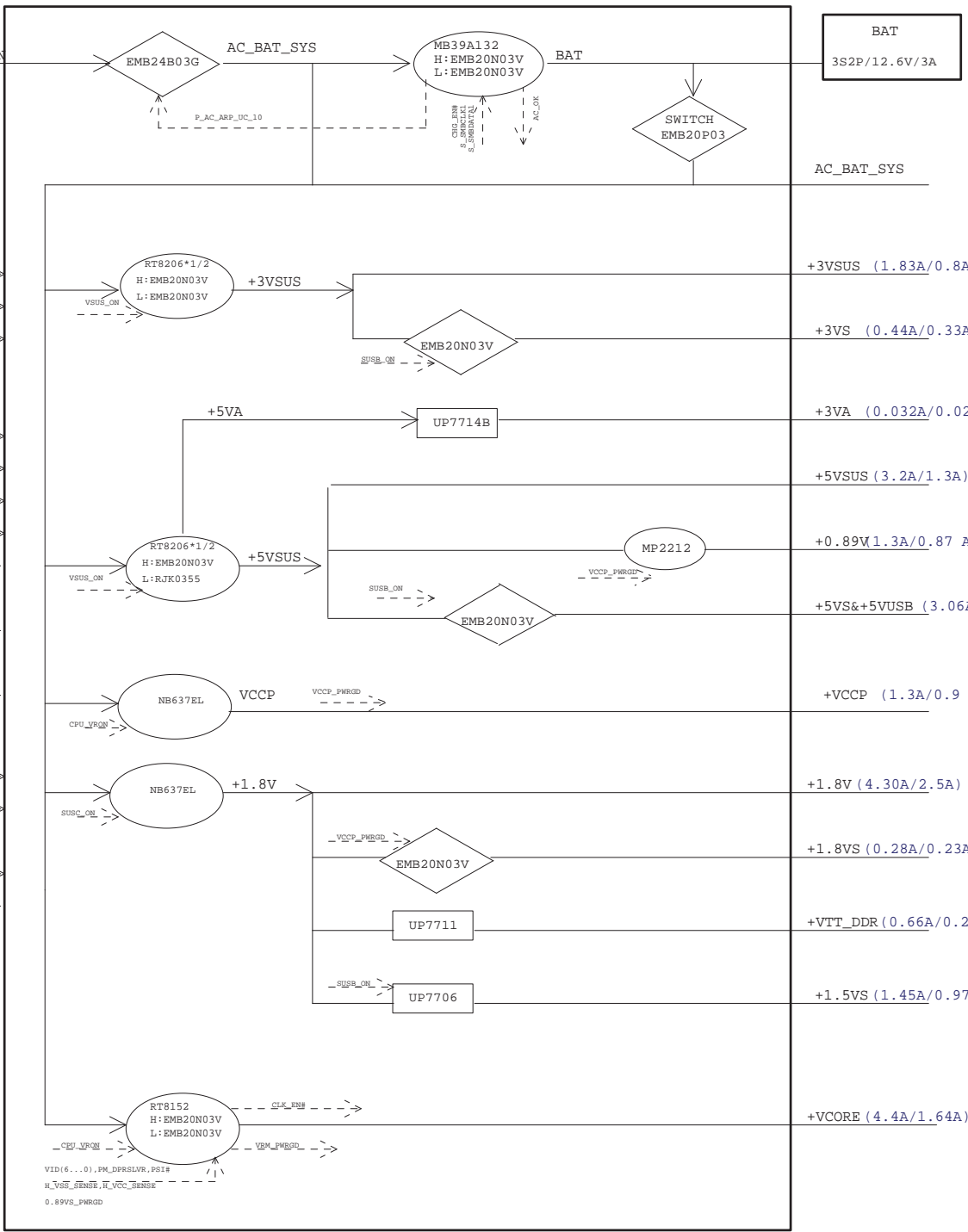
Default Group-1005P SR HIGH END

ASUS		Title : SREW HOLE&EMI	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size A3	Project Name 1015P	Rev 1.2G	
Date: Wednesday, February 24, 2010		Sheet 32 of 42	

Adaptor
40W(19V/2.1A)

EC

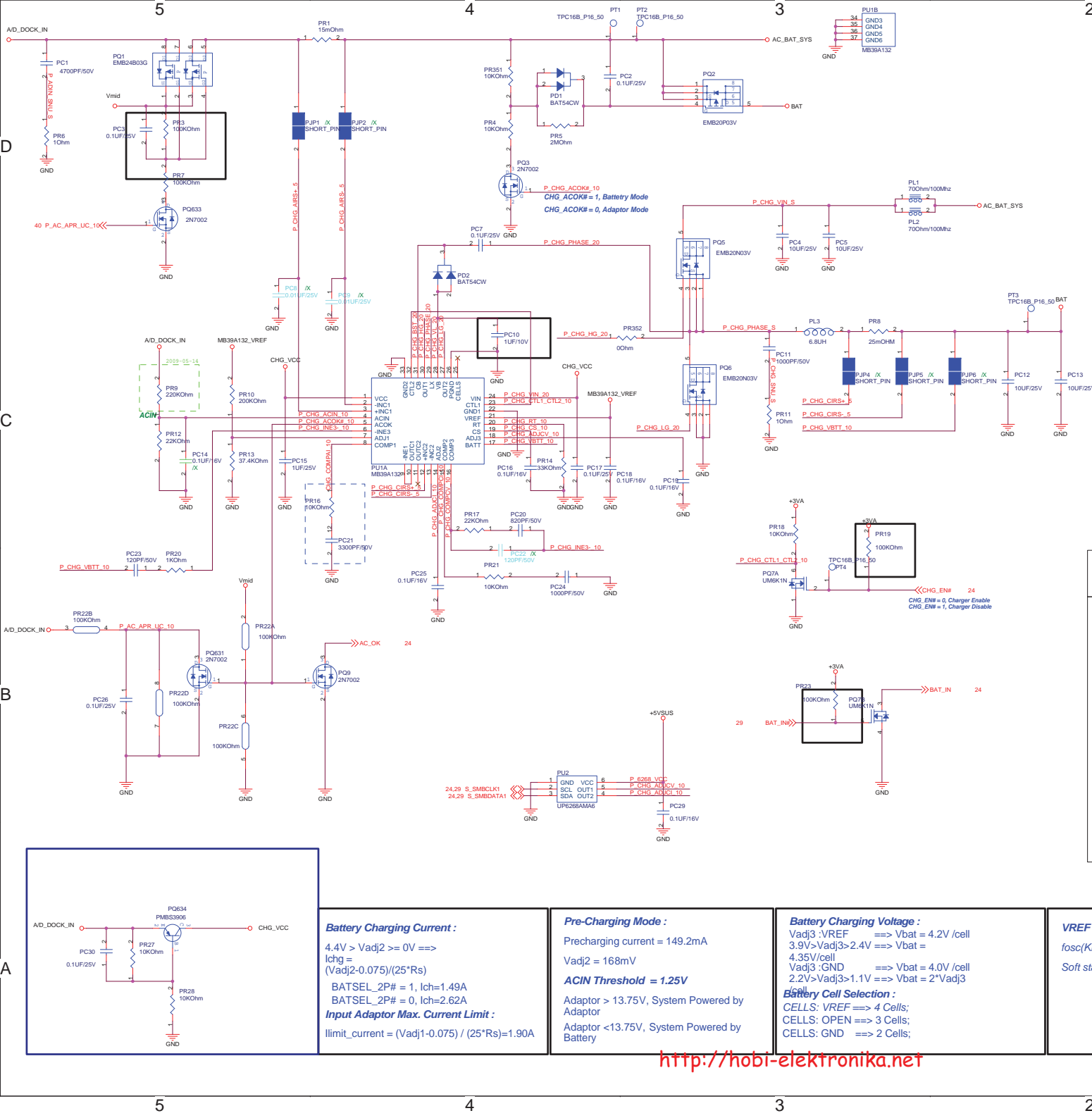
CPU



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STD version :1.02G(09/12/2)

Default Group-1005P SR HIGH END			
		Title : POWER_FLOW	
ASUSTek Computer INC		Engineer:	
Size A2	Project Name 1015P	Rev 1.0	
Date: Wednesday, February 24, 2010		Sheet	33 of 42



Power stage

1. I/P Current:

$$I_{in} = V_o * I_o / (0.8 * V_{in}) = 1.64A$$

2. Ripple Current:

$$I_{rip} = 1.18A$$

$$I_{spec} = 2A \times 1$$

$$pcs$$

3. Inductor Spec:

$$I_{sat} = 10A$$

$$I_{dc} = 5.5A$$

$$DCR = 37m\Omega$$

4. MOSFET Spec:

H-side MOSFET: SI7326DN_T1_E3

$$R_{ds(ON)} = 22m\Omega \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 6.5A \quad (T = 25^\circ C)$$

$$I_{peak} = 40A \quad (\text{Pause} < 10\mu s)$$

L-side MOSFET: SI7326DN_T1_E3

$$R_{ds(ON)} = 22m\Omega \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 6.5A \quad (T = 25^\circ C)$$

$$I_{peak} = 40A \quad (\text{Pause} < 10\mu s)$$

Controller

1. Voltage & Current:

$$+12.6V @ 2.5A$$

2. Frequency:

$$PR122 = 33K\Omega, \quad f_{osc} = 515KHz$$

3. OCP:

4. POR:

$$POR \text{ Hysteresis} = 0.1V$$

$$V_{on} = 7.5V$$

5. Enable Voltage:

$$V = 2.9V$$

6. Soft start time:

$$T_{ss} = 23ms$$

7. Phase selection:

$$N/A$$

8. Inrush Current:

$$C_{total} = 20\mu F$$

$$I_{inrush} =$$

$$0.01A$$

Battery Charging Current :

$$4.4V > V_{adj2} \geq 0V \Rightarrow$$

$$I_{chg} =$$

$$(V_{adj2} - 0.075) / (25 * R_s)$$

$$BATSEL_2P\# = 1, I_{ch} = 1.49A$$

$$BATSEL_2P\# = 0, I_{ch} = 2.62A$$

Input Adaptor Max. Current Limit :

$$I_{limit_current} = (V_{adj1} - 0.075) / (25 * R_s) = 1.90A$$

Pre-Charging Mode :

$$\text{Precharging current} = 149.2mA$$

$$V_{adj2} = 168mV$$

ACIN Threshold = 1.25V

$$\text{Adaptor} > 13.75V, \text{ System Powered by}$$

$$\text{Adaptor}$$

$$\text{Adaptor} < 13.75V, \text{ System Powered by}$$

$$\text{Battery}$$

Battery Charging Voltage :

$$V_{adj3} : V_{REF} \Rightarrow V_{bat} = 4.2V / \text{cell}$$

$$3.9V > V_{adj3} > 2.4V \Rightarrow V_{bat} =$$

$$4.35V / \text{cell}$$

$$V_{adj3} : GND \Rightarrow V_{bat} = 4.0V / \text{cell}$$

$$2.2V > V_{adj3} > 1.1V \Rightarrow V_{bat} = 2 * V_{adj3}$$

Battery Cell Selection :

$$\text{CELLS: } V_{REF} \Rightarrow 4 \text{ Cells;}$$

$$\text{CELLS: OPEN} \Rightarrow 3 \text{ Cells;}$$

$$\text{CELLS: GND} \Rightarrow 2 \text{ Cells;}$$

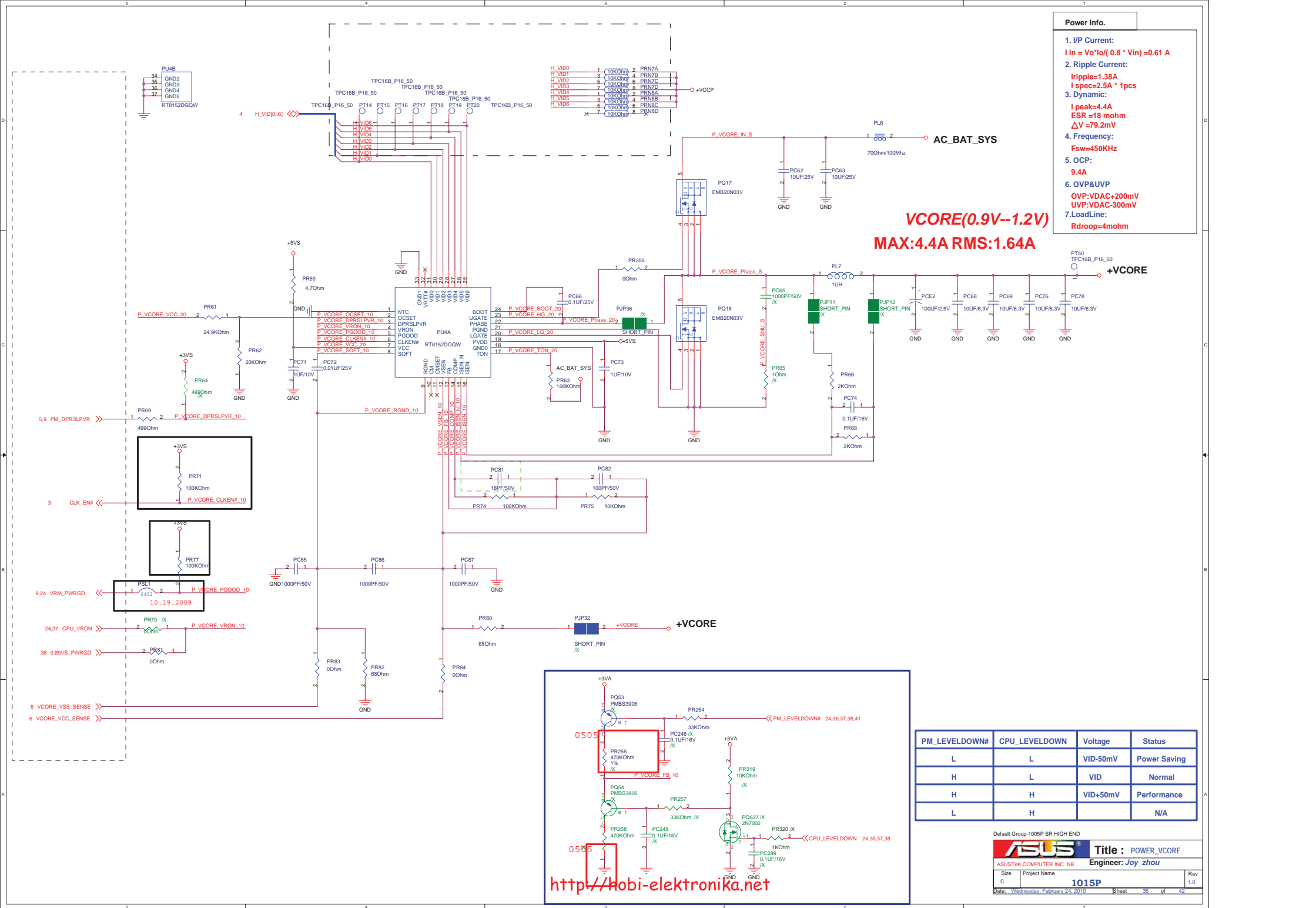
VREF = 5.0V

$$f_{osc}(KHz) = 17000 / RT (K\Omega)$$

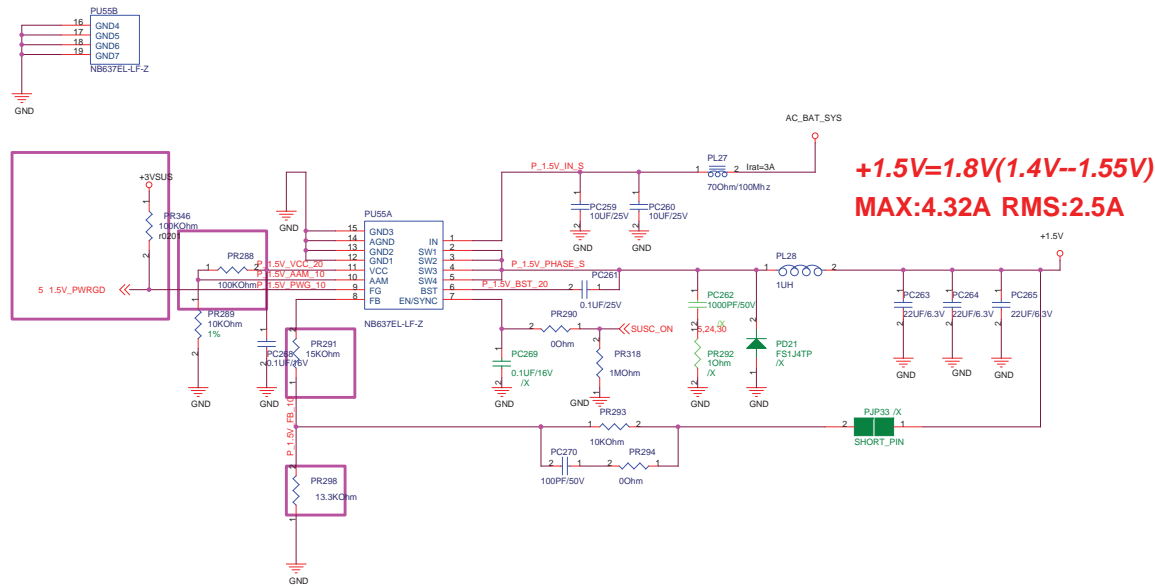
$$\text{Soft start: } t_s(s) = 0.13 * C_{UF} (uF)$$

Default Group:1005P SR HIGH END

ASUS		Title : Charger	
ASUSTek Computer INC		Engineer: Joy_Zhou	
Size	Project Name	Rev	<RevCode>
A2	1008P		
Date: Wednesday, February 24, 2010		Sheet	34 of 42



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Power Info.

- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.08A$
- Ripple Current:**
 $I_{rip} = 1A$
- Frequency:**
 $F_{osc} = 600KHz$
- Current Limit:**
6A

0.9VS@1A

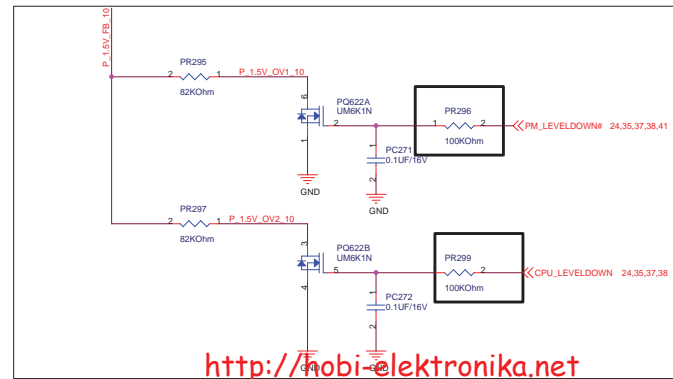
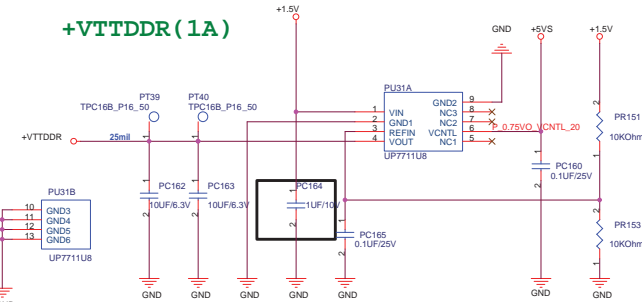
- Dropout Voltage:**
 $\Delta V = 0.3V \quad (I_o = 2A)$
- Current Limit:**
 $I_{limit} = 4A$
- Continue Current:**
 $I_{cont} = 3A$
- Power Dissipation:**
 $R_{thjc} = 52 \text{ } ^\circ C/W$
 $P_d = 1.9W$

2009.11.27

\llcorner SUSC_ON 5.24.30
 \llcorner PM_LEVELDOWN# 24.35.37.38.41
 \llcorner CPU_LEVELDOWN 24.35.37.38

PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.670V	Power Saving
H	L	H	1.800V	Normal
H	H	L	1.912V	Performance
L	H	L		

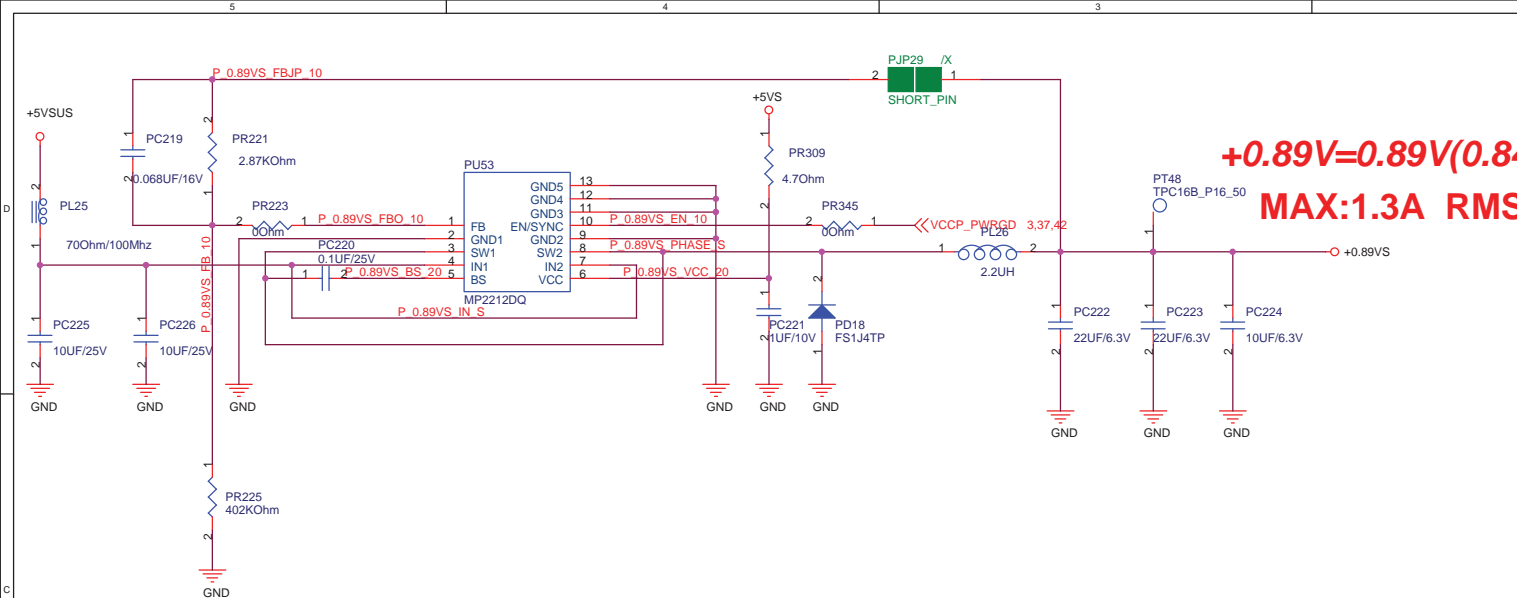
+VTTDDR (1A)



<http://nobi-elektronika.net>

Default Group-1005P SR HIGH END

ASUS		Title : +1.8V&VTTDDR	
ASUSTek Computer INC		Engineer: Joy_Zhou	
Size	Project Name	Rev	
Custom	1015P	1.0	
Date: Wednesday, February 23, 2010			
Sheet 38 of 42			



+0.89V=0.89V(0.844V--0.95V)
MAX:1.3A RMS:0.87A

Power Info.

1. I/P Current:

$$I_{in} = V_o * I_o / (0.8 * V_{in}) = 0.36A$$

2. Ripple Current:

$$I_{rip} = 0.61A$$

$$I_{spec} = 2.5A * 1pc$$

3. Dynamic:

$$I_{peak} = 1.6A$$

$$ESR = 18 \text{ mohm}$$

$$\Delta V = 28.8mV$$

4. Frequency:

$$F_{osc} = 600KHz$$

5. Current Limit:

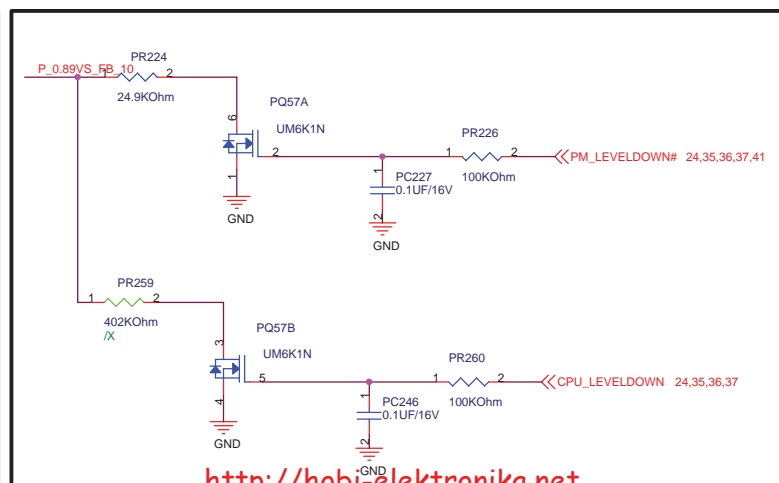
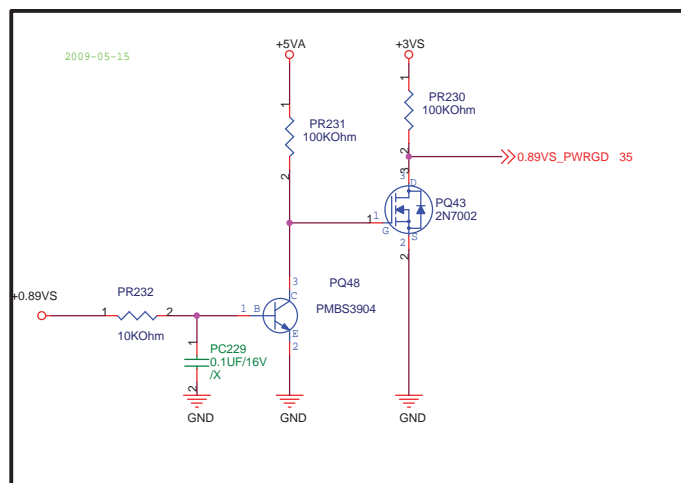
6A

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——— VCCP_PWRGD 3.37,42

——— PM_LEVELDOWN# 24,35,36,37,41

——— CPU_LEVELDOWN 24,35,36,37

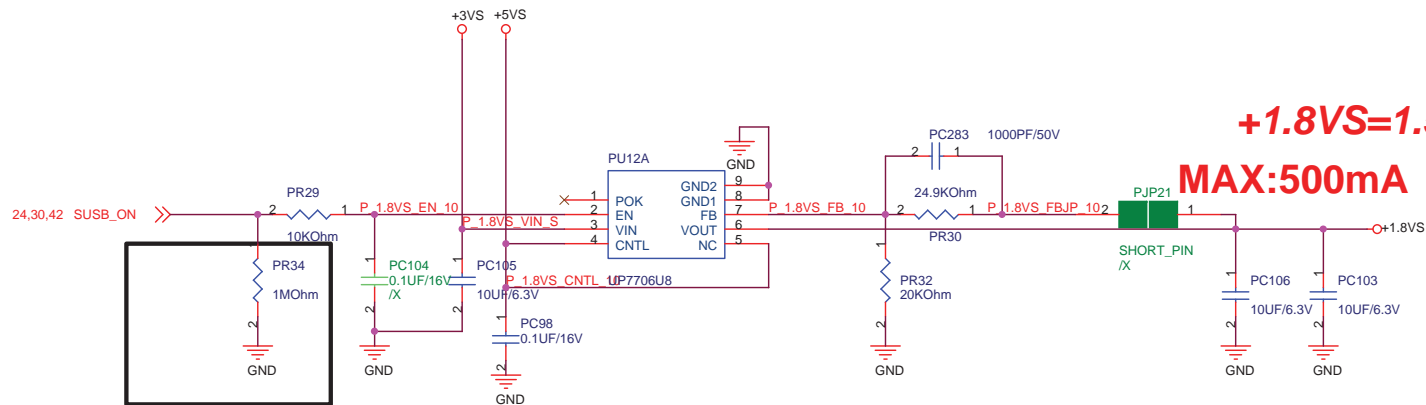


<http://hobi-elektronika.net>

PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage	Status
L	L	0.844V	Power Saving
H	L	0.897V	Normal
H	H	0.950V	Performance
L	H		N/A

Default Group-1005P SR HIGH END

ASUS		Title : +1.5VS & +2.5VS	
ASUSTek Computer INC		Engineer: Joy_Zhou	
Size A3	Project Name 1015P	Rev 1.0	
Date: Wednesday, February 24, 2010		Sheet	38 of 42



1. Dropout Voltage:

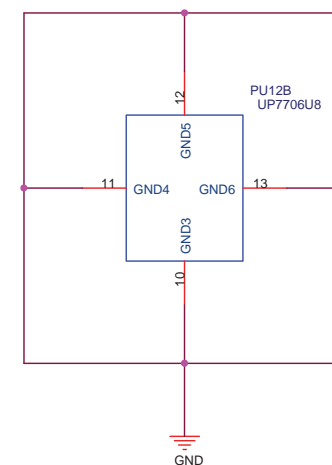
V= 300 mV (I_o=2A)

2. Current Limit:

I limit= 2.8A

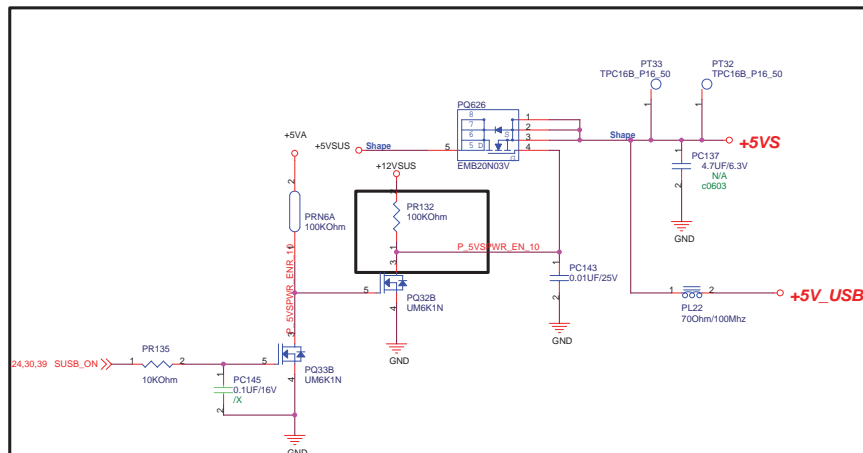
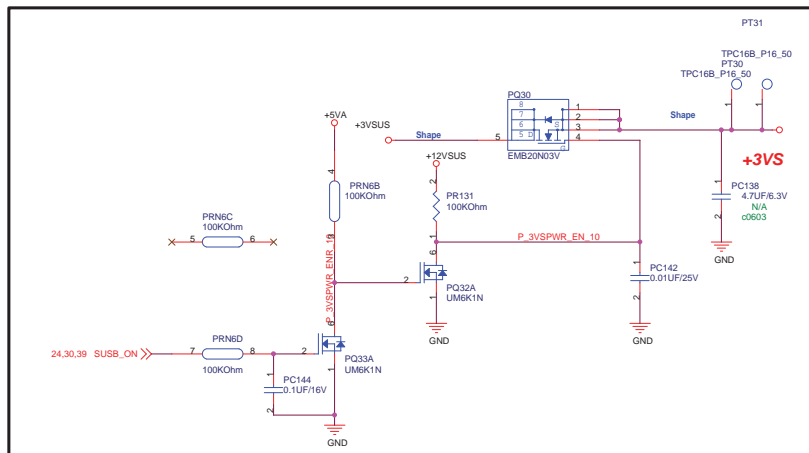
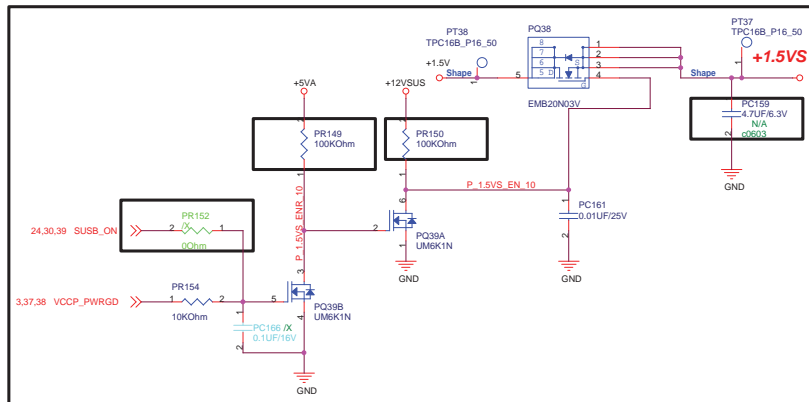
3. Pd:

R thjc =5 C/W
Pd =1.9W



Default Group-1005P SR HIGH END

ASUS		Title : +1.5VS & +2.5VS	
ASUSTek Computer INC		Engineer: <i>Joy Zhou</i>	
Size B	Project Name 1015P		Rev 1.0
Date: Wednesday, February 24, 2010		Sheet 39 of 42	



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—> SUSB_ON 24,30,39

—> VCCP_PWRGD 3,37,38